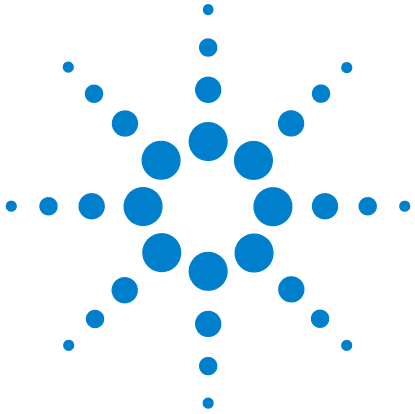

Agilent U7232B DisplayPort Electrical Performance Compliance Test Application

Method of Implementation

Agilent Technologies

Notices

Manual Part Number

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DisplayPort Automated Testing—At A Glance

The Agilent U7232B DisplayPort Electrical Performance Compliance Test Application helps you verify DisplayPort Source device under test (DUT) compliance to DisplayPort specifications using an Agilent Infiniium digital storage oscilloscope. The DisplayPort Electrical Performance Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the DisplayPort Electrical Performance Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Compliance testing measurements are described in Section 3, Source Compliance Tests, in the *DisplayPort- Compliance Test Specification Version 1.2* document, which complies to the *DisplayPort Standards 1.1a* and *1.2*. For more information, see the VESA web site at www.vesa.org.

Required Equipment and Software

In order to run the DisplayPort automated tests, you need the following equipment and software:

- 80000/90000/90000X series Infiniium Digital Storage Oscilloscope (for Compliance Test Specifications 1.1a and below).
- 90000/90000X series Infiniium Digital Storage Oscilloscope (for Compliance Test Specifications 1.2).
- The minimum version of Infiniium oscilloscope software (see the U7232B test application release notes).
- U7232B DisplayPort Electrical Performance Compliance Test Application.
- W2641A/W2641B DisplayPort Test Point Adapter fixture. Includes four SMA to SMP cables.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable for calibrating the oscilloscope.
- E2655A/B probe de-skew fixture.
- E2678A socketed probe.
- E2697A high impedance adapter.
- 1168A or 1169A probes and N5380A SMA probe head.
- U7232B DisplayPort Electrical Performance Compliance Test Application license.
- N5400A EZJIT Plus Jitter Analysis software license.
- N5461A Equalization software license (required for CTS 1.2).
- N5465A InfiniiSim software license (required for CTS 1.2).

In order to run the DisplayPort source automated tests, you need the following additional hardware:

- W2642A DisplayPort Test Controller (DPTC).
- Quantum Data DisplayPort Adapter.

In This Book

This manual describes the tests that are performed by the DisplayPort Electrical Performance Compliance Test Application in more detail; it contains information from (and refers to) the *DisplayPort Specification Version 1.2*, and it describes how the tests are performed.

- Chapter 1, "Installing the DisplayPort Electrical Performance Compliance Test Application" shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the DisplayPort Electrical Performance Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, "Source Eye Diagram Differential Tests" shows the probing and test procedure of the source data eye diagram differential tests.
- Chapter 4, "Source Total Jitter Differential Tests" shows the probing and test procedure of the source total jitter differential tests.
- Chapter 5, "Source Non-ISI Jitter Differential Tests" shows the probing and test procedure of the source non-isi jitter differential tests.
- Chapter 6, "Source Random Jitter Differential Tests" shows the probing and test procedure of the source random jitter differential tests.
- Chapter 7, "Source Transition Time Differential Tests (Informative)" describes the source rise time and fall time differential tests. These are informative tests.
- Chapter 8, "Source Non Pre-Emphasis Level Differential Tests" describes the source non Pre-Emphasis level differential tests.
- Chapter 9, "Source Overshoot Differential Tests (Informative)" shows the probing and test procedure of the source overshoot differential tests. These are informative tests.
- Chapter 10, "Source Pre-Emphasis Level Differential Tests (Normative & Informative)" shows the probing and test procedure of the source pre-Emphasis differential tests. The Pre-Emphasis Level tests are normative tests whereas Non-Transition Voltage Range Measurements are informative tests.
- Chapter 11, "Source PostCursor 2 Verification Tests (Normative)" shows the probing and test procedure of the source PostCursor 2 verification tests.
- Chapter 12, "Source Inter Pair Skew Differential Tests" shows the probing and test procedure of the source inter pair skew differential tests.
- Chapter 13, "Source Unit Interval Differential Tests (Informative)" describes the source unit interval differential tests. These are informative tests.

- Chapter 14, “Source Main Link Frequency Compliance Differential Tests” shows the probing and test procedure of the source main link frequency compliance differential tests.
- Chapter 15, “Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)” describes the source spread spectrum clocking (SSC) differential tests. In this SSC test, the Modulation Frequency and Modulation Deviation tests are normative tests whereas Deviation HF Variation tests are informative tests.
- Chapter 16, “Source Rise-Fall Mismatch Single-Ended Tests (Informative)” shows the probing and test procedure of the source rise and fall mismatch single-ended tests.
- Chapter 17, “Source Intra Pair Skew Single-Ended Tests” shows the probing and test procedure of the source intra pair skew single-ended tests.
- Chapter 18, “Source AC Common Mode Noise Single-Ended Tests” shows the probing and test procedure of the source AC common mode noise single-ended tests.
- Chapter 19, “Link Layer Phy Change Tests” describes the link layer phy change tests.
- Chapter 20, “Sink Eye Diagram Tests” shows the probing and test procedure of the sink eye diagram tests.
- Chapter 21, “Sink Total Jitter Tests” contains more information on the sink total jitter tests.
- Chapter 22, “Sink Non-ISI Jitter Tests” shows the probing and test procedure of the sink non-isi jitter tests.
- Chapter 23, “Cable Eye Diagram Tests” shows the probing and test procedure of the cable eye diagram tests.
- Chapter 24, “Cable Total Jitter Tests” contains more information on the cable total jitter tests.
- Chapter 25, “Cable Non-ISI Jitter Tests” contains more information on the cable non-isi jitter tests.
- Chapter 26, “Aux Channel Tests” contains more information on the Aux Channel tests.
- Chapter 27, “Aux Channel Sensitivity Tests” contains more information on the Aux Channel Sensitivity tests.
- Chapter 28, “DP Inrush Tests” contains more information on the DP Inrush tests.
- Chapter 29, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the DisplayPort automated tests.
- Chapter 30, “InfiniiMax Probing” describes the 1168A/1169A probe amplifier and probe head recommendations for DisplayPort testing.

See Also

- The DisplayPort Electrical Performance Compliance Test Application's online help, which describes:
  - Starting the tests.
  - Creating or opening a test project.
  - Setting up the DisplayPort test environment.
  - Setting up the source automated tests with W2642A DPTC.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running the tests.
  - Viewing the test results.
  - Viewing/printing the HTML test report.
  - Saving test projects.
  - Understanding the HTML report.

Contents

1 Installing the DisplayPort Electrical Performance Compliance Test Application

If you purchased the U7232B DisplayPort Electrical Performance Compliance Test Application, you need to install the software and license key.

Installing the Software

1 Make sure you have the minimum version of Infiniium oscilloscope software (see the U7232B test application release notes) by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DisplayPort Electrical Performance Compliance Test Application, go to Agilent website: http://www.agilent.com/find/scope-apps-sw.

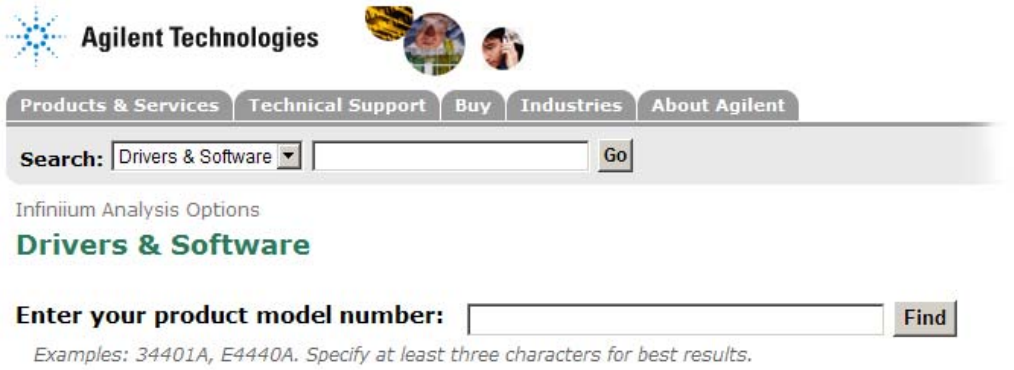


Figure 1 Agilent website for software Downloads

3 Search the list on this web page for the link to the U7232B DisplayPort Electrical Performance Compliance Test Application. Click on it and follow the instructions to download and install the application.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

   You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application to complete the license installation.

1 Installing the DisplayPort Electrical Performance Compliance Test Application

2 Preparing to Take Measurements

Before running the DisplayPort automated tests, you need to acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort Electrical Performance Compliance Test Application and perform the measurements.

W2641A/W2641B DisplayPort Test Point Adapter Fixture

The W2641A/W2641B test fixture is the Agilent DisplayPort test point adapter fixture that is used for all of the DisplayPort compliance tests.

Acquiring the Test Fixture

The W2641A/W2641B DisplayPort test point adapter fixture can be acquired from Agilent Technologies.

W2641A Test Fixture Description

Figure 2 shows the top view of the W2641A test fixture.

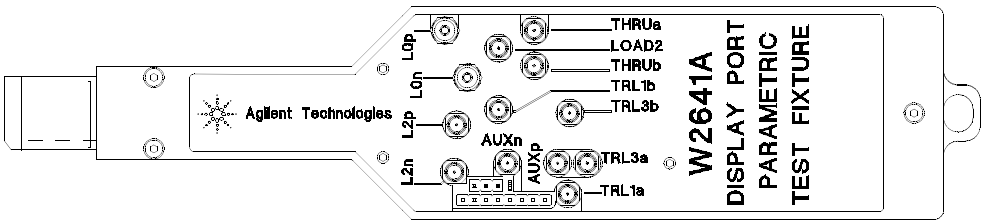


Figure 2 W2641A DisplayPort Test Point Adapter Fixture (Top View)

W2641B Test Fixture Description

Figure 3 shows the top view of the W2641B test fixture.

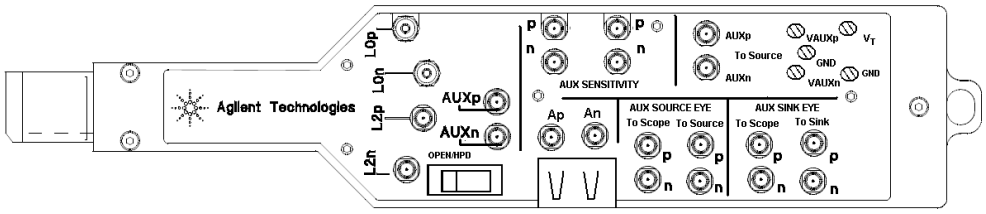


Figure 3 W2641B DisplayPort Test Point Adapter Fixture (Top View)

Calibrating the Oscilloscope

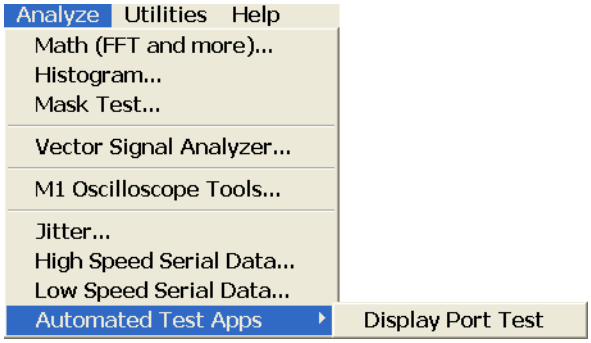
If you haven't already calibrated the oscilloscope and probe, see Chapter 29, "Calibrating the Infiniium Oscilloscope and Probe.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort Electrical Performance Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DisplayPort Test**.



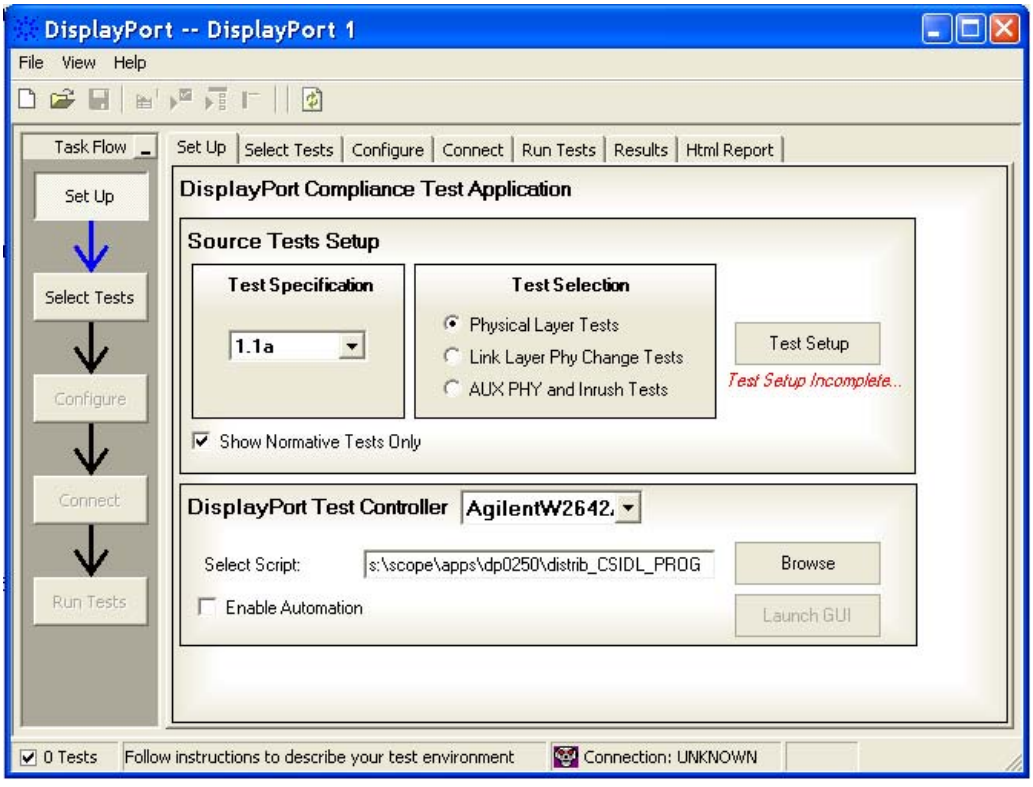


Figure 4 The DisplayPort Electrical Performance Compliance Test Application

NOTE If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort Electrical Performance Compliance Test Application has not been installed (see Chapter 1, "Installing the DisplayPort Electrical Performance Compliance Test Application).

Figure 4 shows the DisplayPort Electrical Performance Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you select your setup options. Allows you to setup by connection type, device identifier, jitter separation measurements and test fixture type.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested and configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DisplayPort application, each channel's probe is configured as single-ended or differential depending on the last DisplayPort test that was run.

Online Help Topics

For information on using the DisplayPort Electrical Performance Compliance Test Application, see the online help (which you can access by choosing **Help>Contents**... from the application's main menu).

The DisplayPort Electrical Performance Compliance Test Application's online help describes:

- Running the Compliance Test Application on a second monitor.
- Starting the DisplayPort Electrical Performance Compliance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DisplayPort test environment.
- Setting up DisplayPort automated tests with W2642A DPTC.
- Selecting the tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running the tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change the display settings.
  - To change the margin thresholds and report trial display.
  - To change the auto-recovery option.
- Viewing or printing the HTML test report.
- Saving the test projects.
- Understanding the DisplayPort HTML report.

3 Source Eye Diagram Differential Tests

This section provides the guidelines for source eye diagram differential tests using an Agilent Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Data Eye Diagram Differential Tests

When performing the data eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 5 and Figure 6 show a physical connection for making differential and single-ended connections.

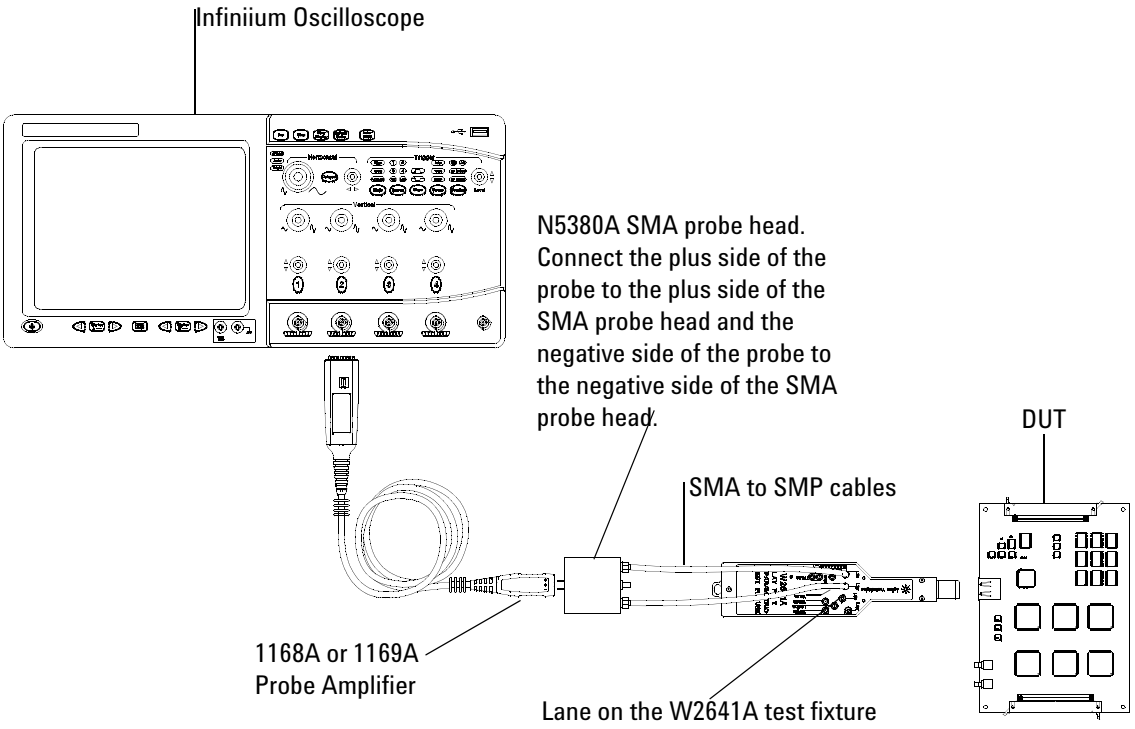


Figure 5 Probing for Differential Tests - Data Eye Diagram Tests (Single Connection with W2641A DisplayPort Test Fixture)

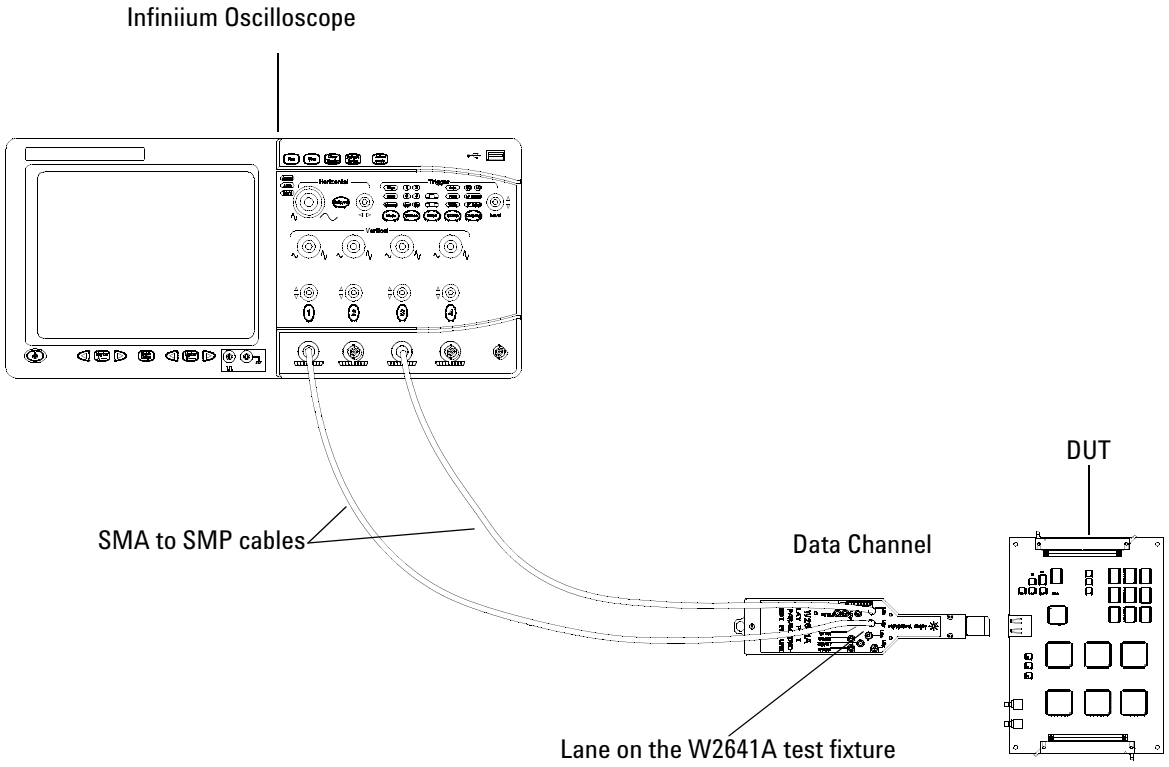


Figure 6 Differential Measurement Setup Using Two Single Ended Connections - Data Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see Chapter 30, “InfiniiMax Probing,” starting on page 299.

Source Eye Diagram Differential Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in transmitted data. The test must use a PRBS 7 test pattern at all voltage levels (for Compliance Test Specifications 1.1a and below) or an 8b10b test pattern (for Compliance Test Specifications 1.2). The test should be performed without pre-Emphasis.

The source eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.

6 In the DisplayPort Compliance Test Application, click the Set Up tab.

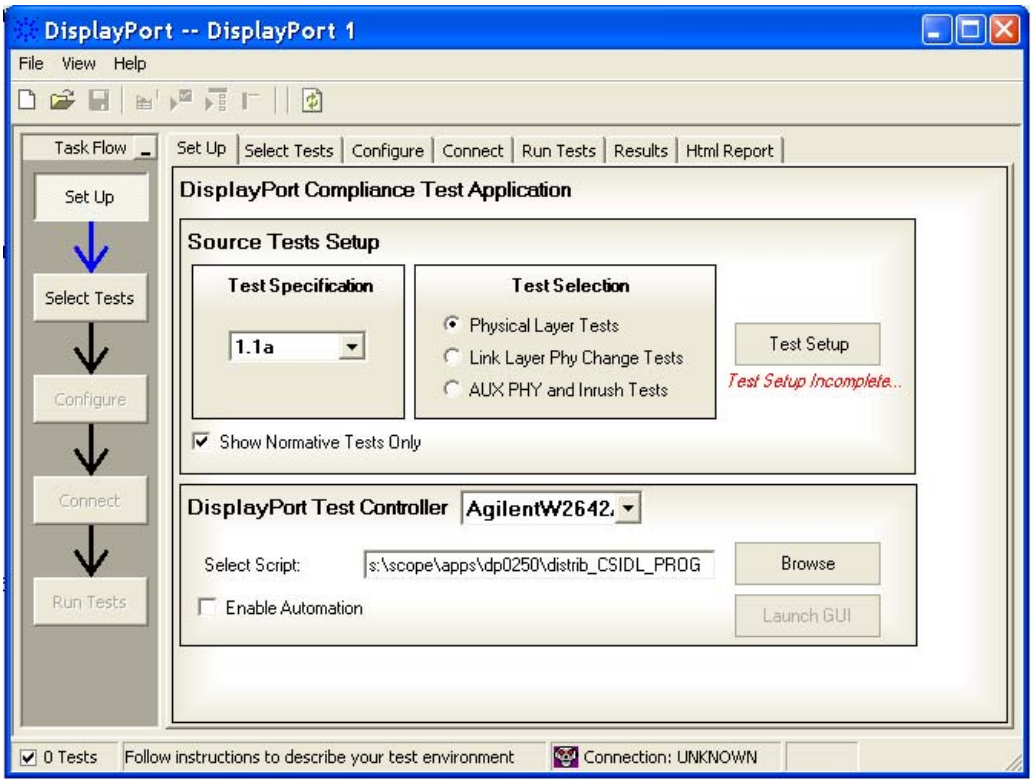


Figure 7 Set Up for Data Eye Pattern Differential Tests

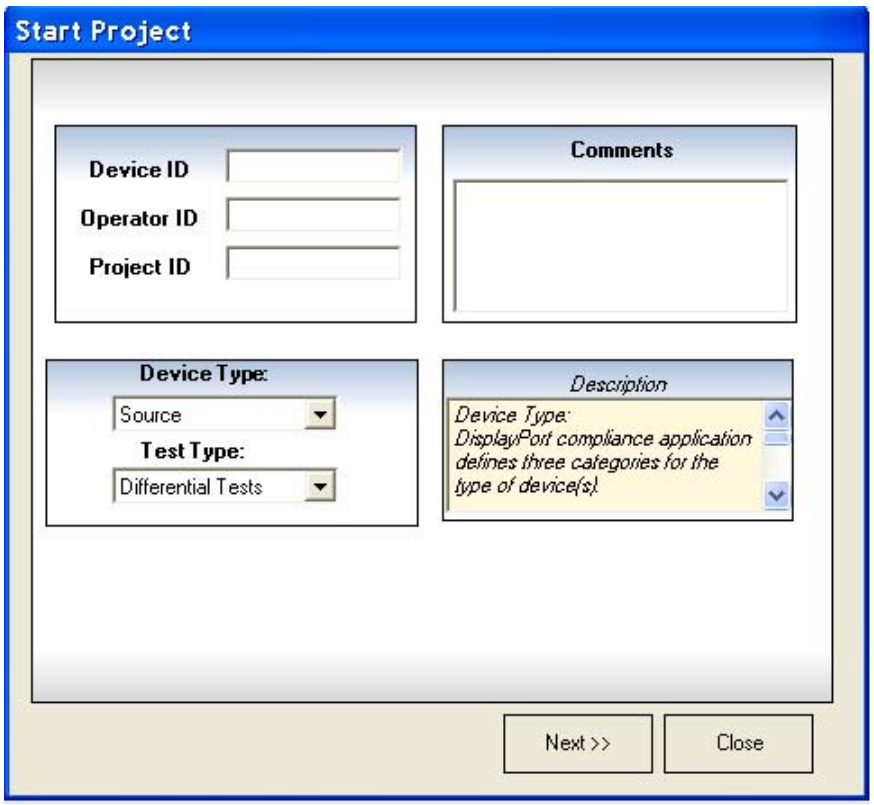


Figure 8 Test Type Set Up for Data Eye Pattern Differential Tests

7 Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Eye Diagram - Lane # - Eye Diagram Test where # is the lane number to be tested.

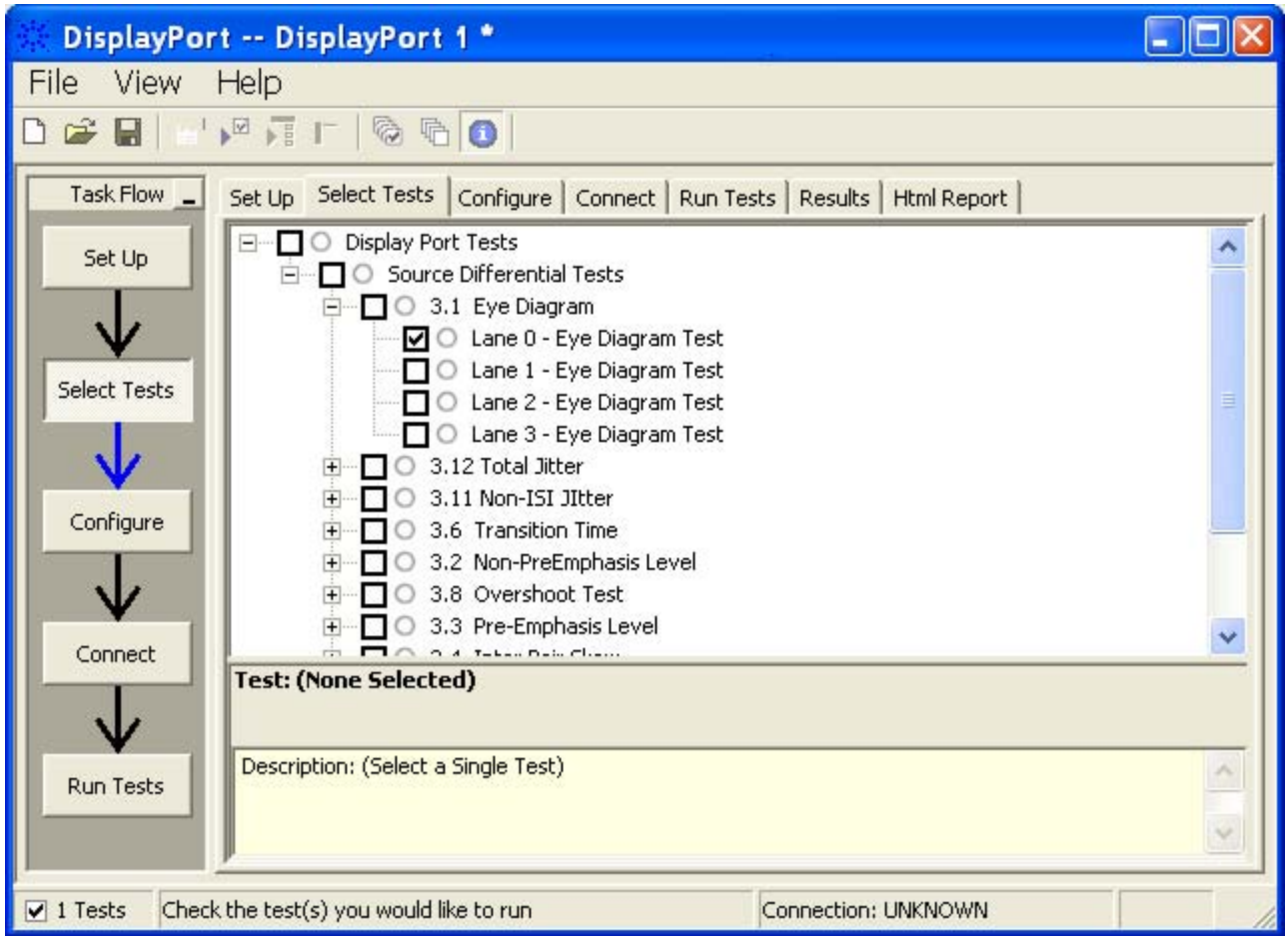


Figure 9 Selecting Data Eye Pattern Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 1), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 1 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 1 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Eye Diagram Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
CTS Version for Eye Mask	Set the mask file to CTS version 1.0, 1.1, or 1.2

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB (for CTS 1.1a and below), or set by the source such that the source will meet the Pass/Fail criteria (for CTS 1.2).

Test Pattern: PRBS 7 (for RBR and HBR), or 8b10b (for HBR2).

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

The following table and figure define the mask for the eye measurements of CTS 1.1a and below. There can be no signal trajectories entering into the mask. Table 2 shows the voltage and time coordinates for the mask used in the eye diagram. The specification states that either 400mV, 600mV, or 800mV setting must pass.

Table 2 Eye Diagram Mask Coordinates

	Bit Rate	
Mask Point	**Reduced (1.62 Gb/s)**	**High (2.7 Gb/s)**
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.875, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

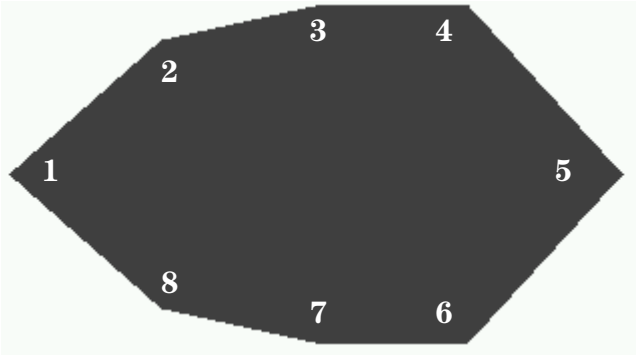


Figure 10 The Source Eye Pattern Mask

Mask Test: Zero mask failures.

For CTS 1.2 eye measurements, there can be no signal trajectories entering the mask area as defined by the following:

Waveform Eye Height: Minimum 124mV

Waveform Eye Width: > .42 UI

The mask is aligned horizontally to the point where the maximum eye height occurs between 0.375UI - 0.625UI. The mask is aligned vertically around 0V differential.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.2 draft8* and Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1a*.

4 Source Total Jitter Differential Tests

This section provides the guidelines for source total jitter differential tests using an Agilent Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Total Jitter Differential Tests

When performing the source total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 11 and Figure 12 show a physical connection for making differential and single-ended connections.

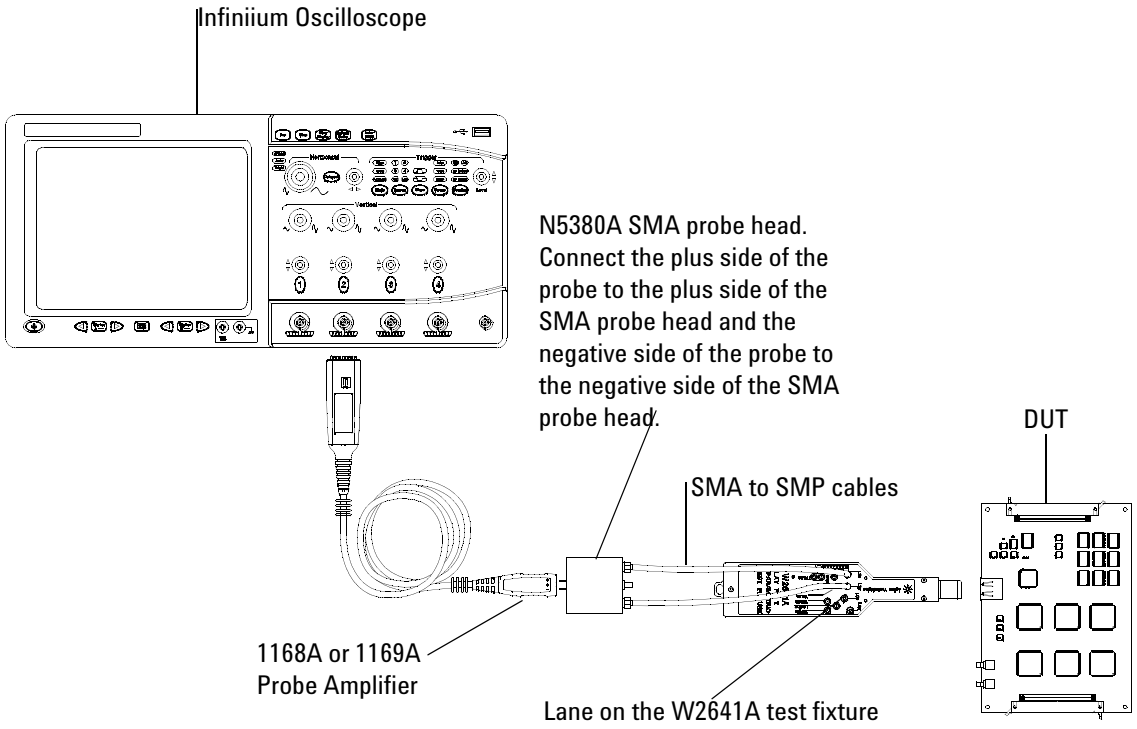


Figure 11 Probing for Differential Tests - Total Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

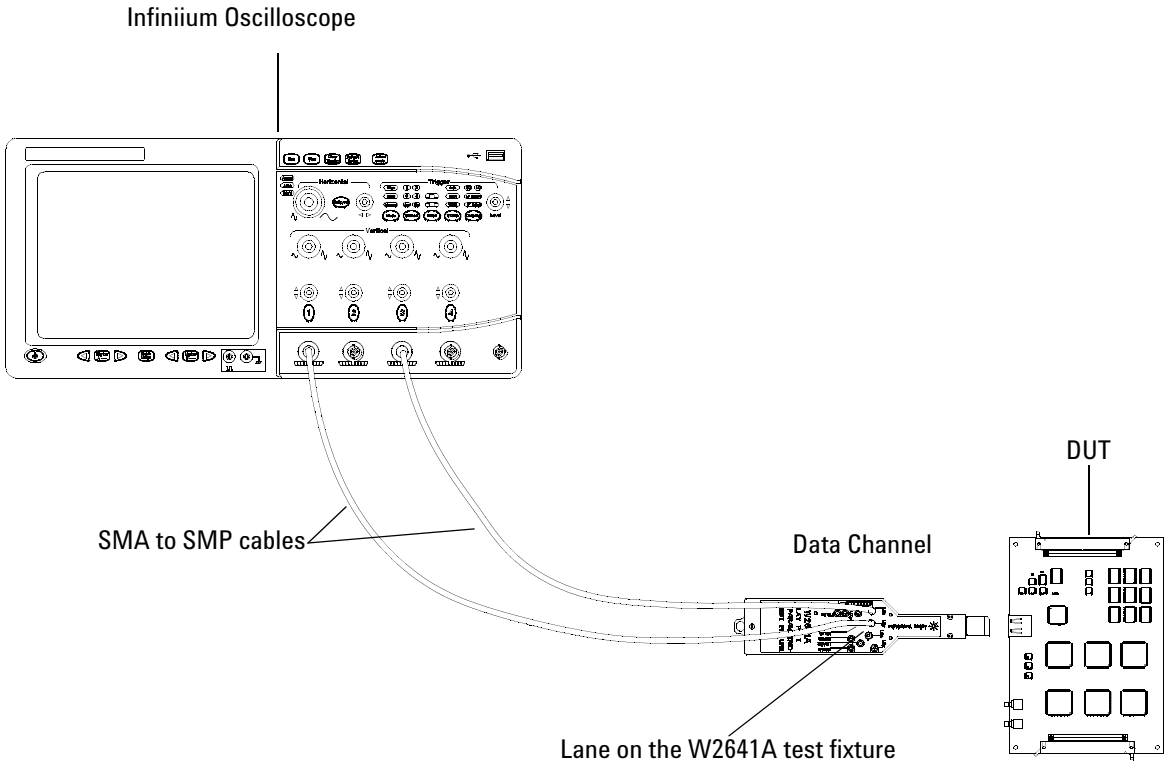


Figure 12 Differential Measurement Setup Using Two Single Ended Connections - Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Total Jitter Differential Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

For Compliance Test Specifications 1.1a and below, the test must use a PRBS 7 test pattern at all voltage levels. For Compliance Test Specifications 1.2, the test must use an 8b10b or a D10.2 test pattern. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Total Jitter - Lane # - where # is the lane number to be tested.

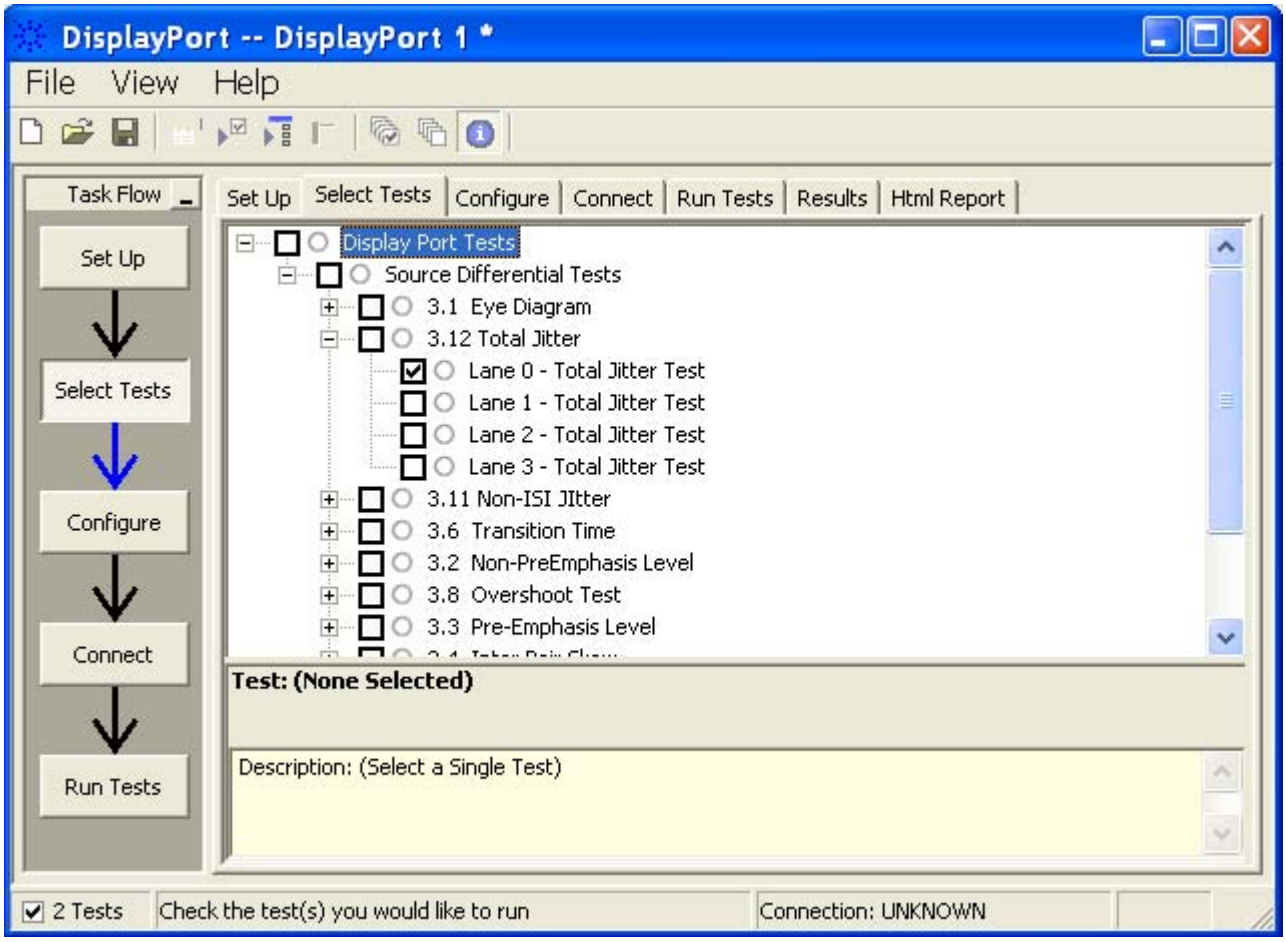


Figure 13 Selecting Source Total Jitter Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 3), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 3 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.

Table 3 Test Configuration Options

Configuration Option	Description
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.

Test Condition

Bit Rate: all bit rates are supported (for CTS 1.1a and below), or 5.4Gbps (for CTS 1.2).

Output Level: all output levels are supported (for CTS 1.1a and below), or user-defined (for CTS 1.2).

Pre-Emphasis: 0 dB (for CTS 1.1a and below), or user-defined (for CTS 1.2).

Test Pattern: PRBS 7 (for RBR and HBR), or 8b10b and D10.2 (for HBR2).

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Table 4 Total Jitter at Internal and Compliance Points (CTS 1.1a).

	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)	
A_{p-p}	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)	
A_{p-p}	0.270 UI

Table 5 Total Jitter at Internal and Compliance Points (CTS 1.2).

	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)	
A_{p-p}	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)	
A_{p-p}	0.270 UI

Receiver Connector (TP3_EQ)		
High-bit Rate 2 (5.4 Gb/s per lane)		
	8b10b	**D10.2**
A_{p-p}	< 0.62 UI	< 0.40 UI

UI is Unit Interval.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.2 draft8* and Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1a*.

5 Source Non-ISI Jitter Differential Tests

This section provides the guidelines for source non-ISI jitter differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Non-ISI Jitter Differential Tests

When performing the non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 14 and Figure 15 show a physical connection for making differential and single-ended connections.

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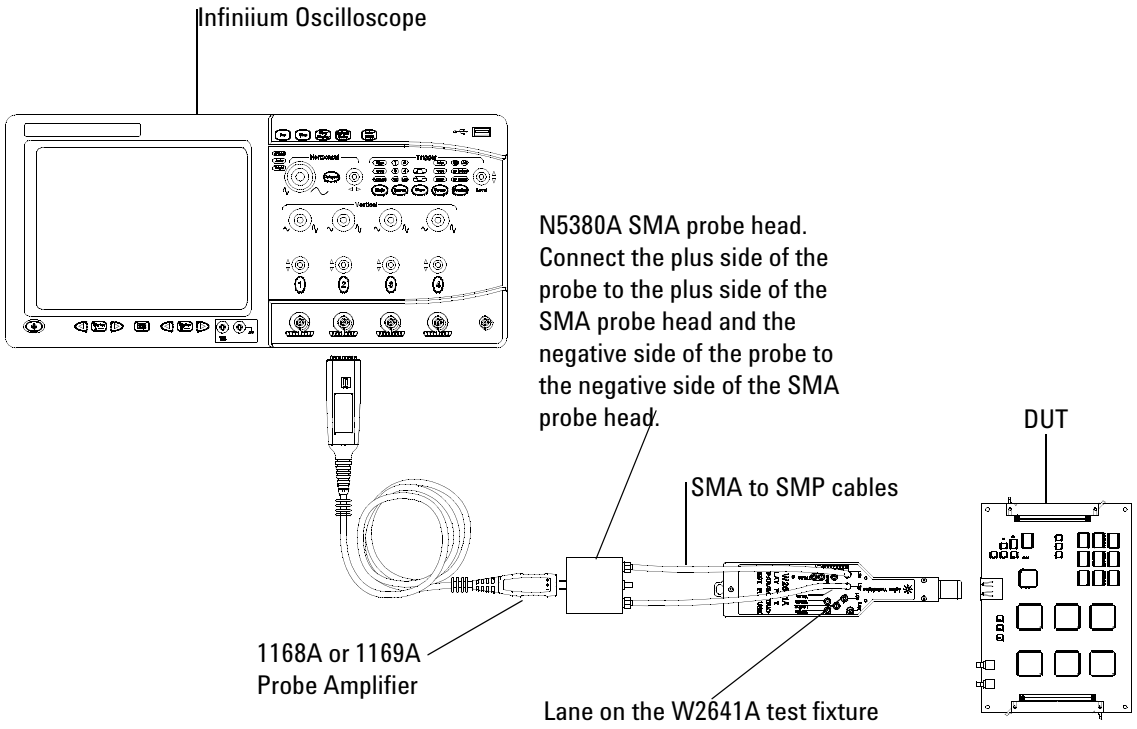

Figure 14 Probing for Differential Tests - Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

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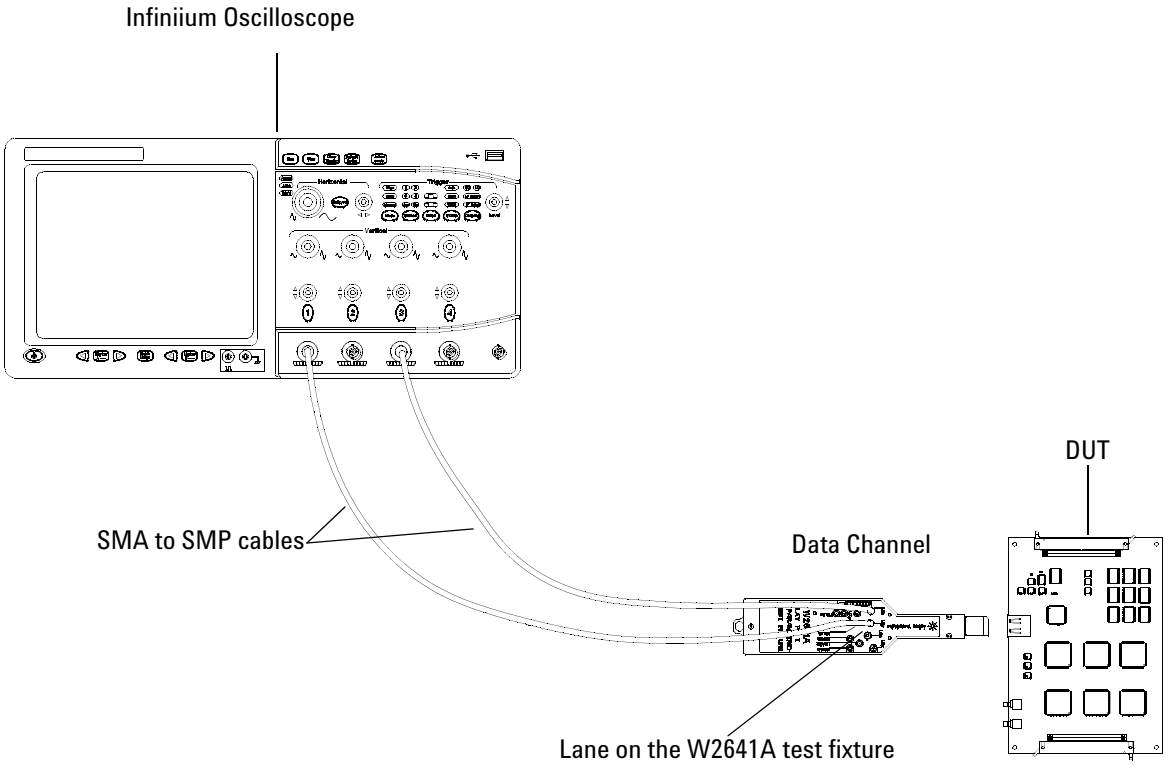

Figure 15 Differential Measurement Setup Using Two Single Ended Connections - Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Non-ISI Jitter Differential Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Non-ISI Jitter - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

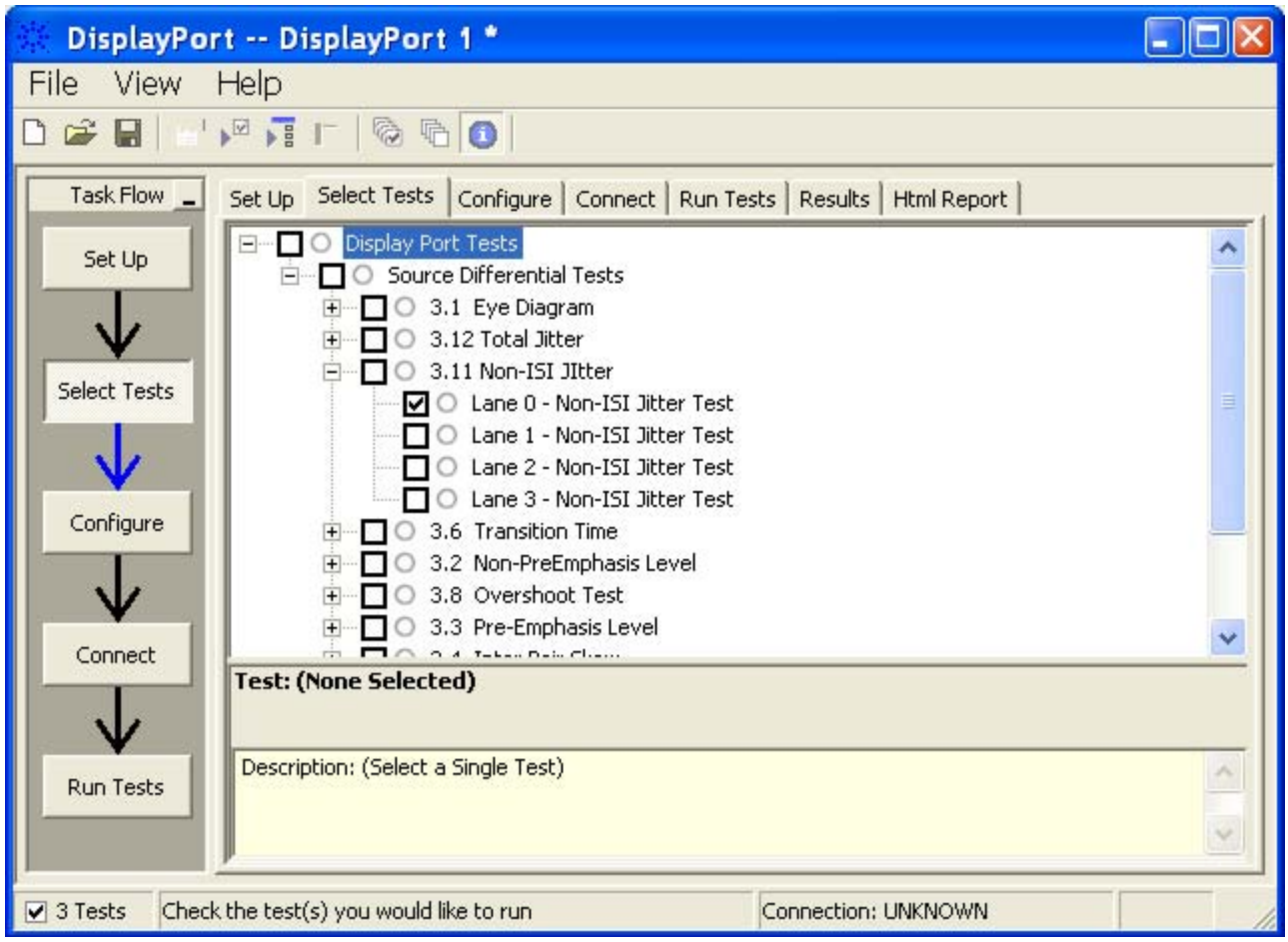

Figure 16 Selecting Source Non-Jitter Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 6), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 6 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.

Table 6 Test Configuration Options

Configuration Option	Description
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Table 7 Non-ISI Jitter at Internal and Compliance Points (CTS 1.1a).

	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)	
A_{p-p}	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)	
A_{p-p}	0.210 UI

Table 8 Non-ISI Jitter at Internal and Compliance Points (CTS 1.2).

	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)	
A_{p-p}	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)	
A_{p-p}	0.170 UI

UI is Unit Interval.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.2 draft8* and Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1a*.

6 Source Random Jitter Differential Tests

This section provides the guidelines for source random jitter differential tests using an Agilent Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Random Jitter Differential Tests

When performing the source random jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 17 and Figure 18 show a physical connection for making differential and single-ended connections.

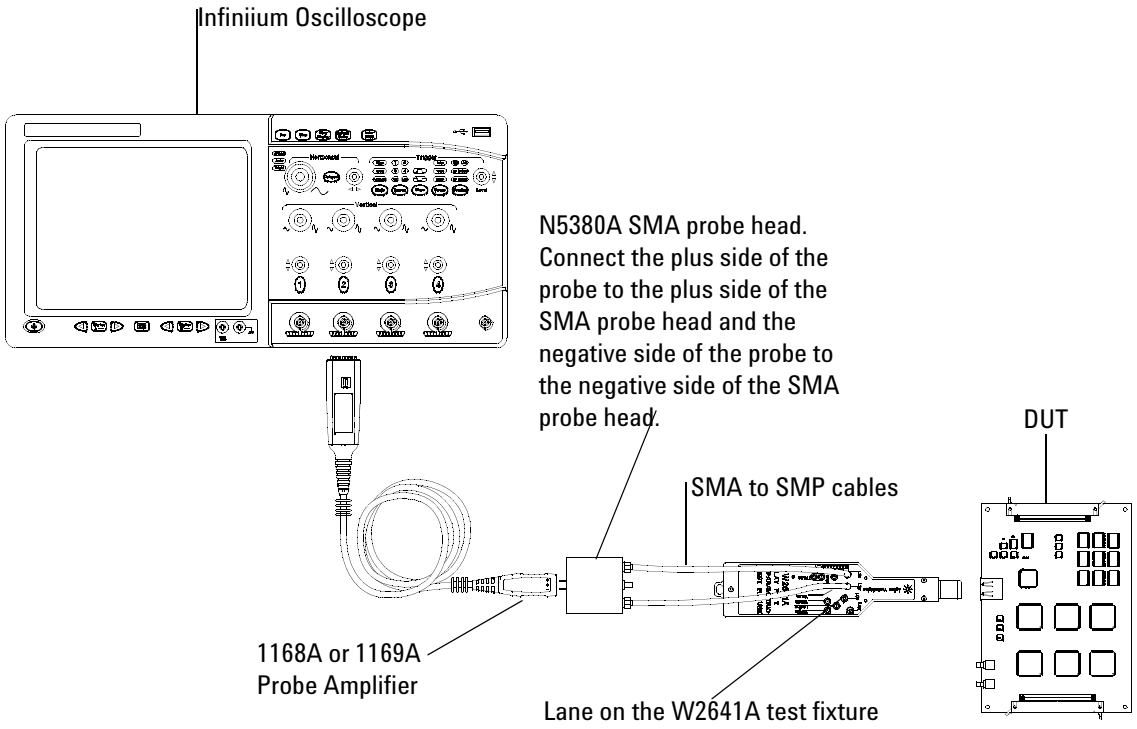

Figure 17 Probing for Differential Tests - Random Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

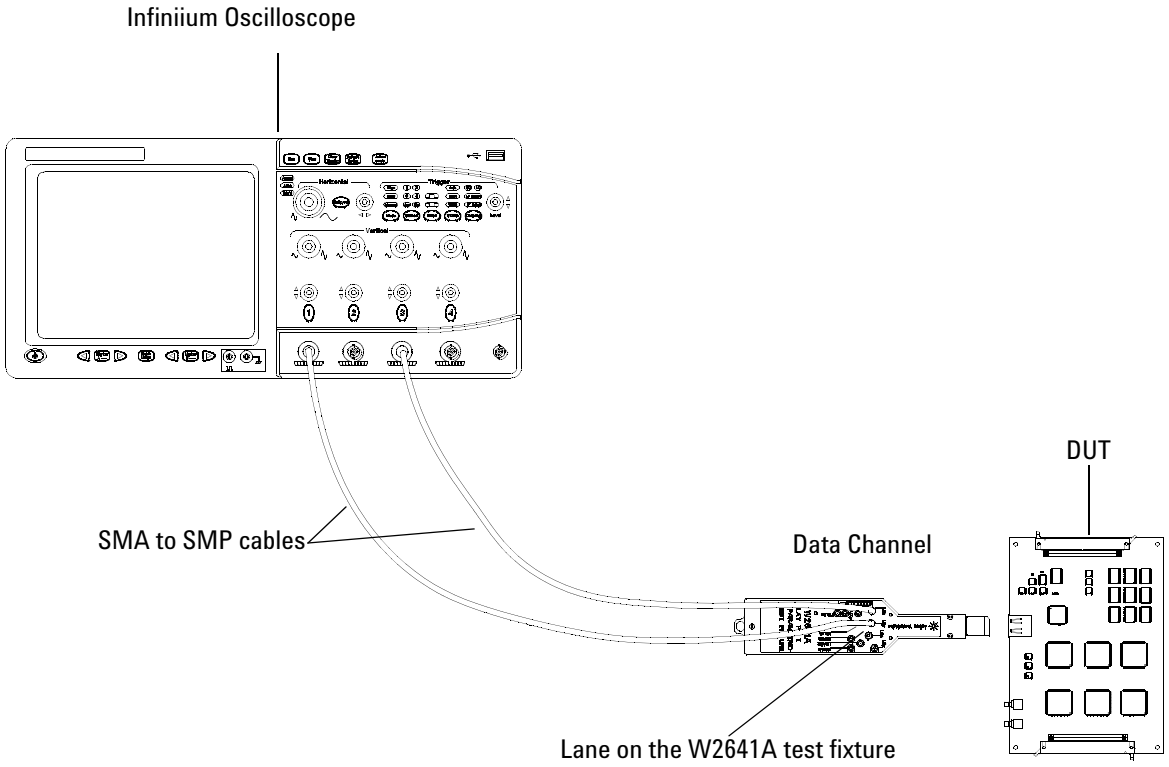

Figure 18 Differential Measurement Setup Using Two Single Ended Connections - Random Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Random Jitter Differential Tests

To evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3-19 VESA DisplayPort Standard 1.2).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in VESA DisplayPort Standard 1.2, Section 9.3: The Dual Dirac Jitter Model).

The test must use an 8b10b or a D10.2 test pattern. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to “3.12 Random Jitter(TP3_EQ) - D10.2”.

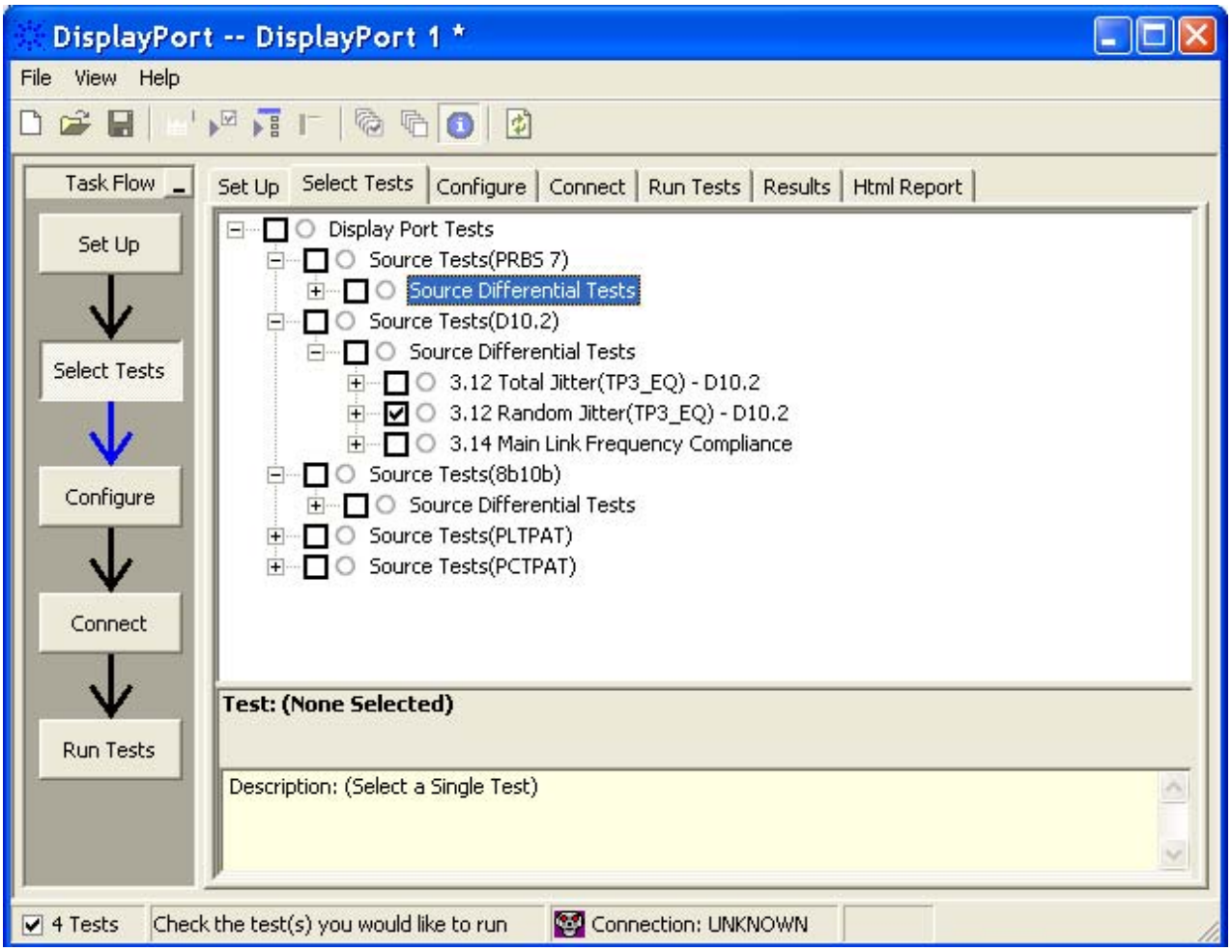

Figure 19 Selecting Source Random Jitter Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options (see Table 9), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 9 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Source Differential Tests	
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.

Test Condition

Bit Rate: 5.4Gbps.

Output Level: User-defined.

Pre-Emphasis: User-defined.

Test Pattern: 8b10b and D10.2.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Table 10 Random Jitter at Internal and Compliance Points.

	Receiver Connector (TP3_EQ)
High-bit Rate 2 (5.4 Gb/s per lane)	
	D10.2
RJ	< 0.23 UI

UI is Unit Interval.

Test References

See Test 3.12: Random Jitter (RJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.2*.

6 Source Random Jitter Differential Tests

7 Source Transition Time Differential Tests (Informative)

This section provides the guidelines for source transition time differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Transition Time Differential Tests

When performing the transition time test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 20 and Figure 21 below show the differential and the single-ended connections for Transition Time Diffential Tests.

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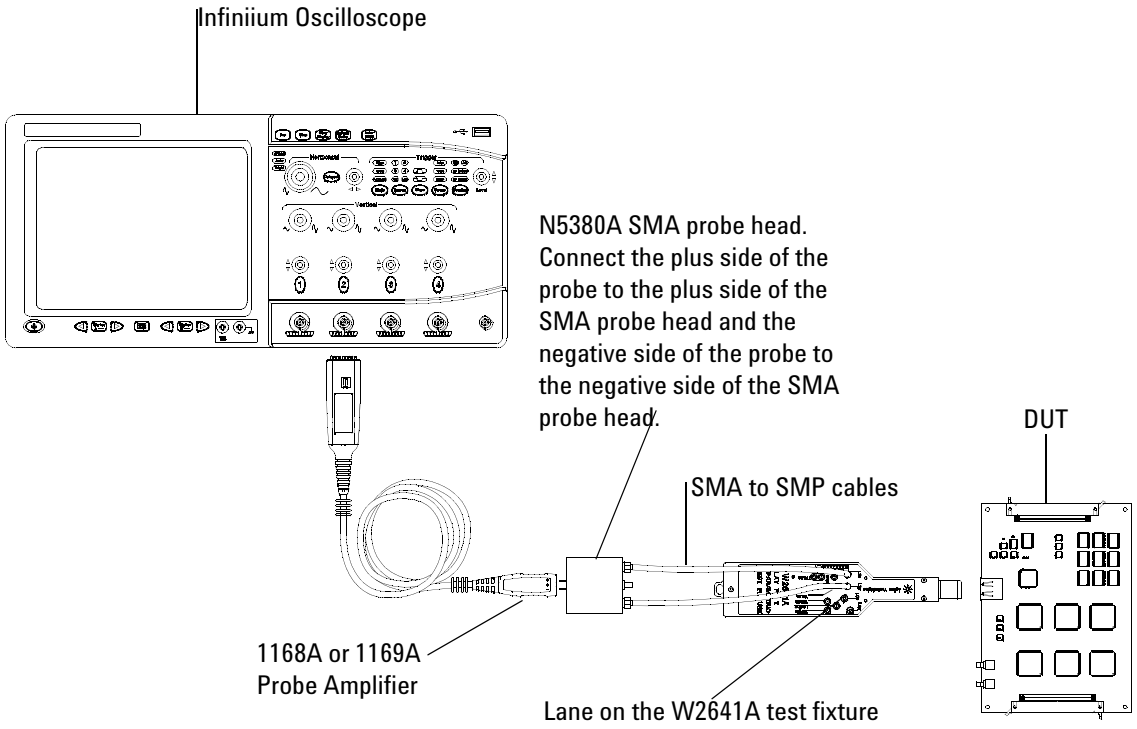

Figure 20 Probing for Differential Tests - Transition Time Tests (Single Connection with W2641A DisplayPort Test Fixture)

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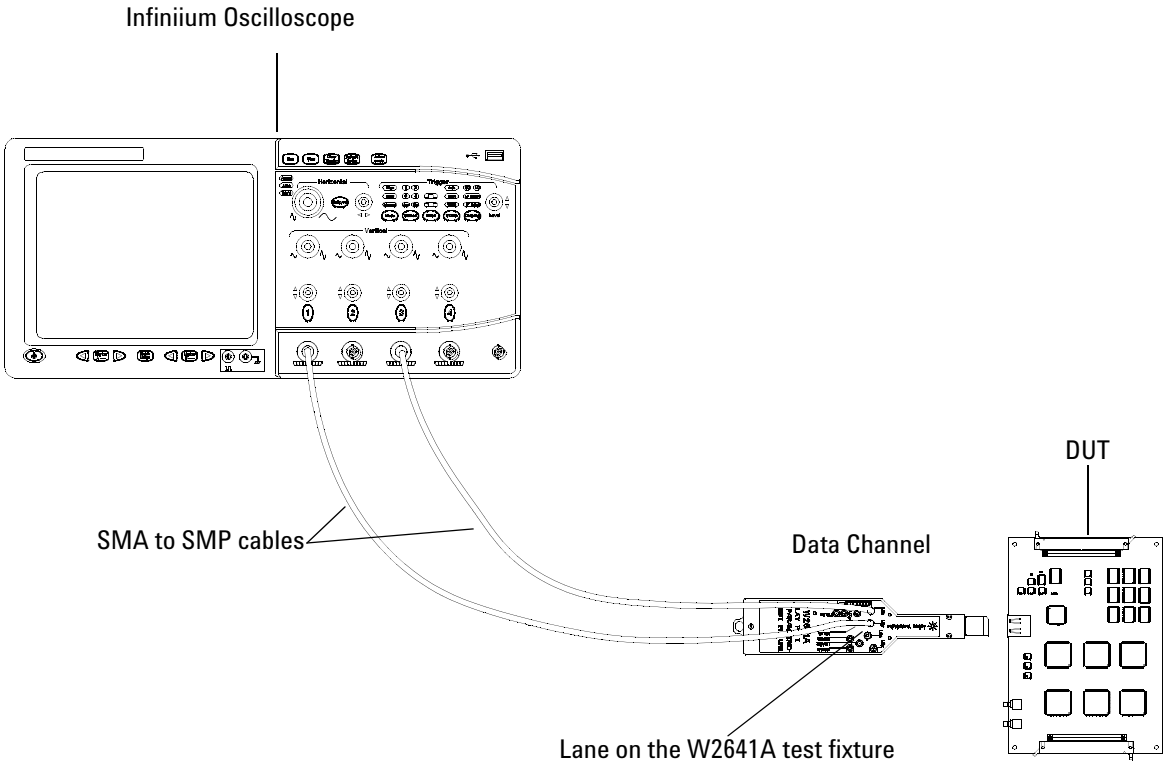

Figure 21 Differential Measurement Setup Using Two Single Ended Connections - Transition Time Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Transition Time Differential Tests

Transition time testing measures the rise time and fall time across the outputs of a differential data lane. The transition is defined as the time interval between the normalized 20% and 80% amplitude levels.

The transition time test should be performed at all bit rates supported without pre-Emphasis for 400 mV differential voltage swing. The source pattern should be a PRBS 7 waveform. This applies to one, two, and four lane operation with all functional lanes being tested. (Reference: Table 3.10 VESA DisplayPort Standard).

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.
8. This is an Informative test, therefore, the Show Normative Tests Only checkbox must be un-checked.

Navigate to the Transition Time group, and check the rise time and fall time tests that you want to perform.

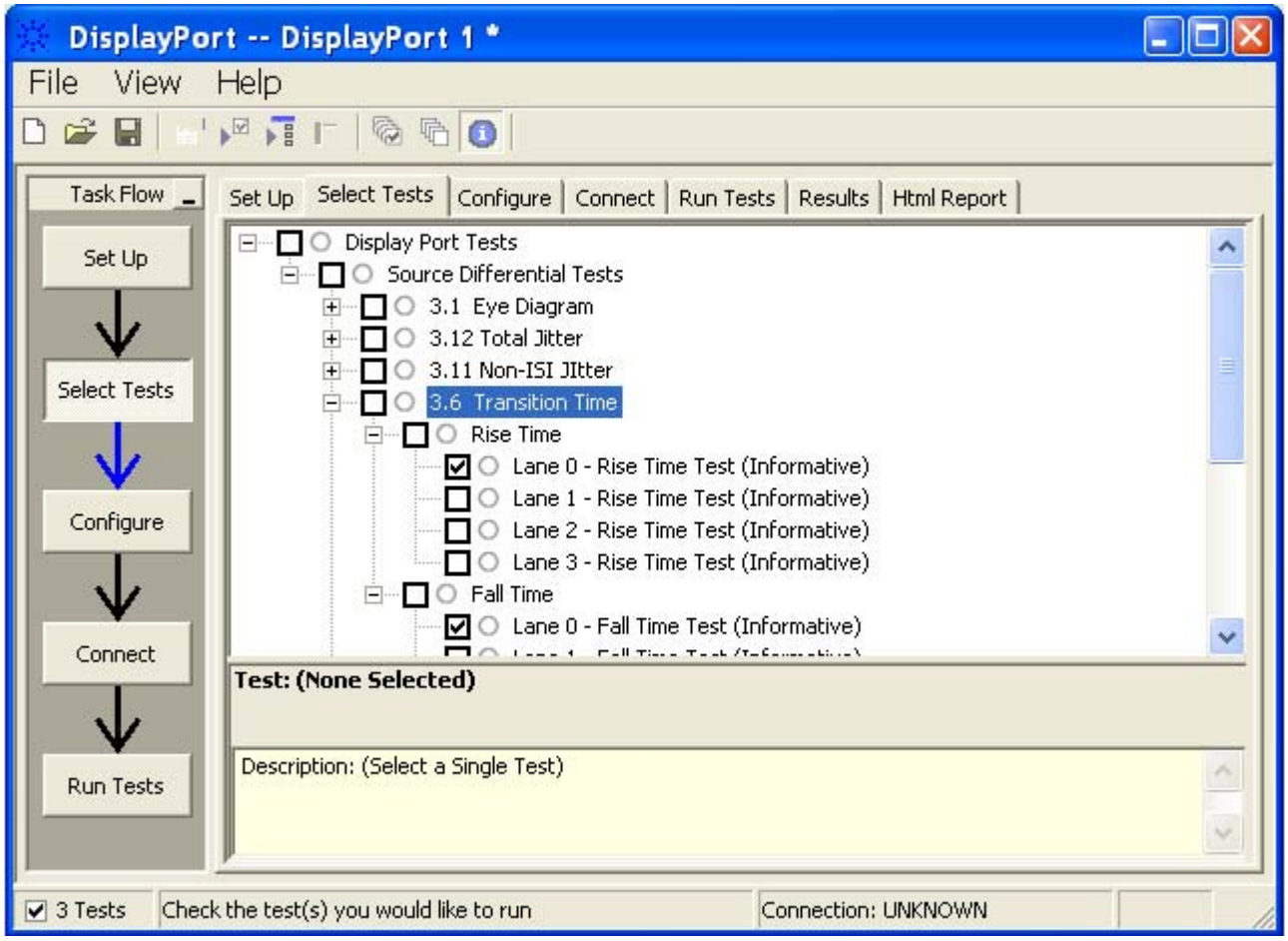

Figure 22 Selecting Transition Time Differential Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 11), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 11 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.

Table 11 Test Configuration Options

Configuration Option	Description
Transition VH Pattern	Sets the pattern for rise time measurement to either 01111, 0111 or 011. The default setting is 0111.
Transition VL Pattern	Sets the pattern for fall time measurement to either 10000, 1000 or 100. The default setting is 1000.
Threshold	Specifies the threshold in percentage.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

50 ps ≤ Transition Time ≤ 160 ps

Test References

See section 3.6, in the *DisplayPort- Compliance Test Specification Version 1.1*.

7 Source Transition Time Differential Tests (Informative)

8 Source Non Pre-Emphasis Level Differential Tests

This section provides the guidelines for source non pre-Emphasis level differential tests using an Agilent Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Non Pre-Emphasis Level Differential Tests

When performing the non pre-Emphasis level differential test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 23 and Figure 24 below show the differential and the single-ended connections for Non Pre-Emphasis Level Differential Tests.

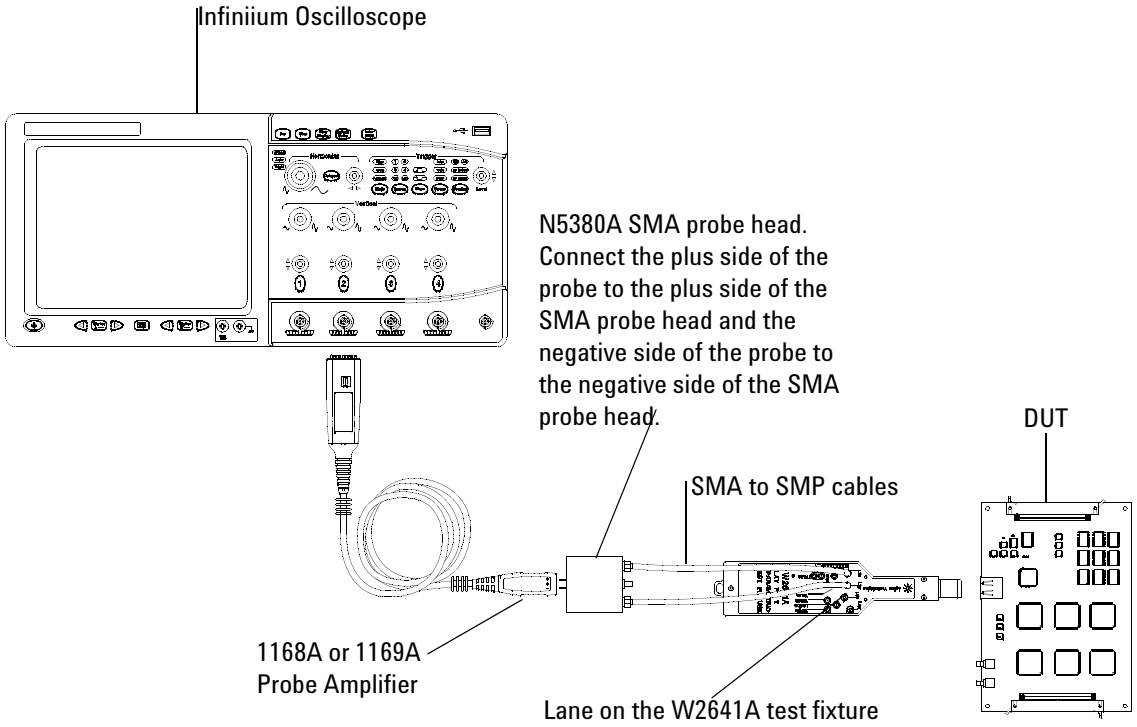

Figure 23 Probing for Differential Tests - Non Pre-Emphasis Level Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

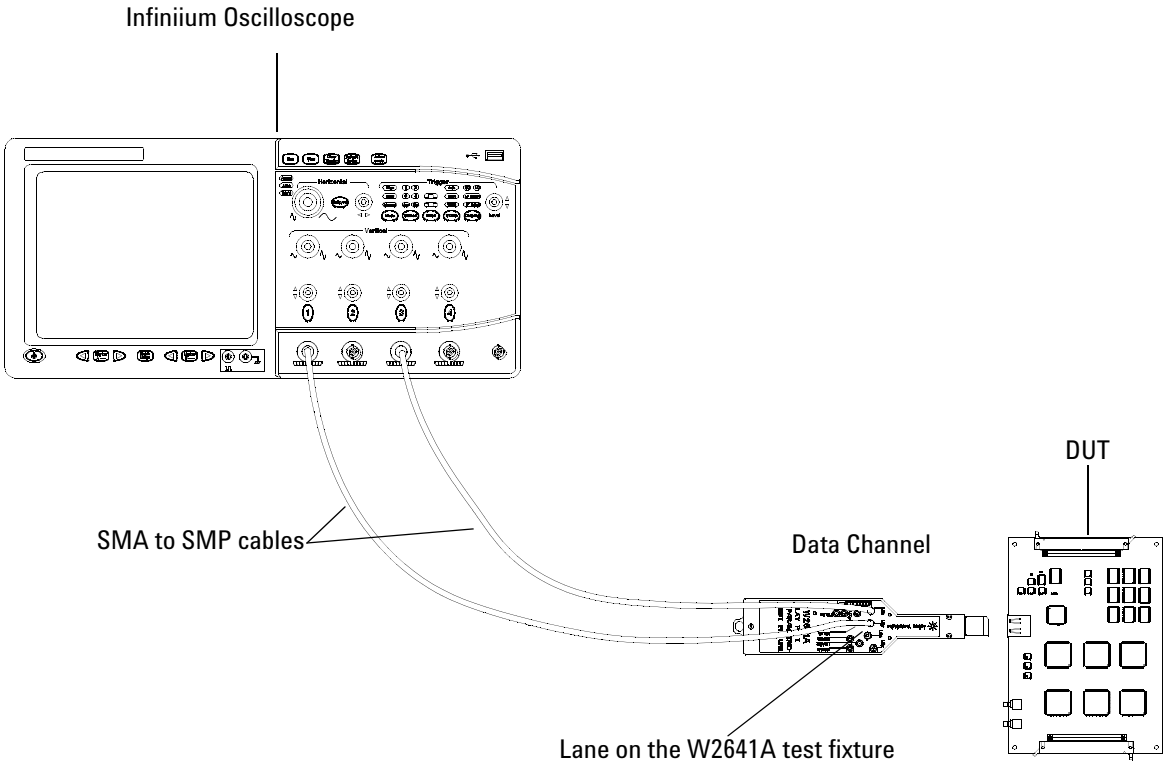

Figure 24 Differential Measurement Setup Using Two Single Ended Connections - Non Pre-Emphasis Level Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Non Pre-Emphasis Level Test

To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven. (Reference: Table 3.10 VESA DisplayPort Standard).

The source is given a range of expected output for each level setting that correlates with the system budget elements such as cable loss and receiver eye minimum and max values. This test ensures that the system budget is obeyed.

For Compliance Test Specifications 1.1a and below, the amplitude measurement is performed at all bit rates without pre-Emphasis and a PRBS 7 waveform. For Compliance Test Specifications 1.2, the amplitude measurement is performed at a bit rate of 5.4Gbps without pre-Emphasis using an 80 bit custom pattern (1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000).

The following equation is used to calculate the measurement result:

$$\text{Peak-to-peak Voltage} = V_H - V_L$$

where:

V_H is the high voltage level
V_L is the low voltage level

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

8 Navigate to the Non-Pre-Emphasis Level - Lane # - Non Pre-Emphasis Level Test where # is the lane number to be tested.

.

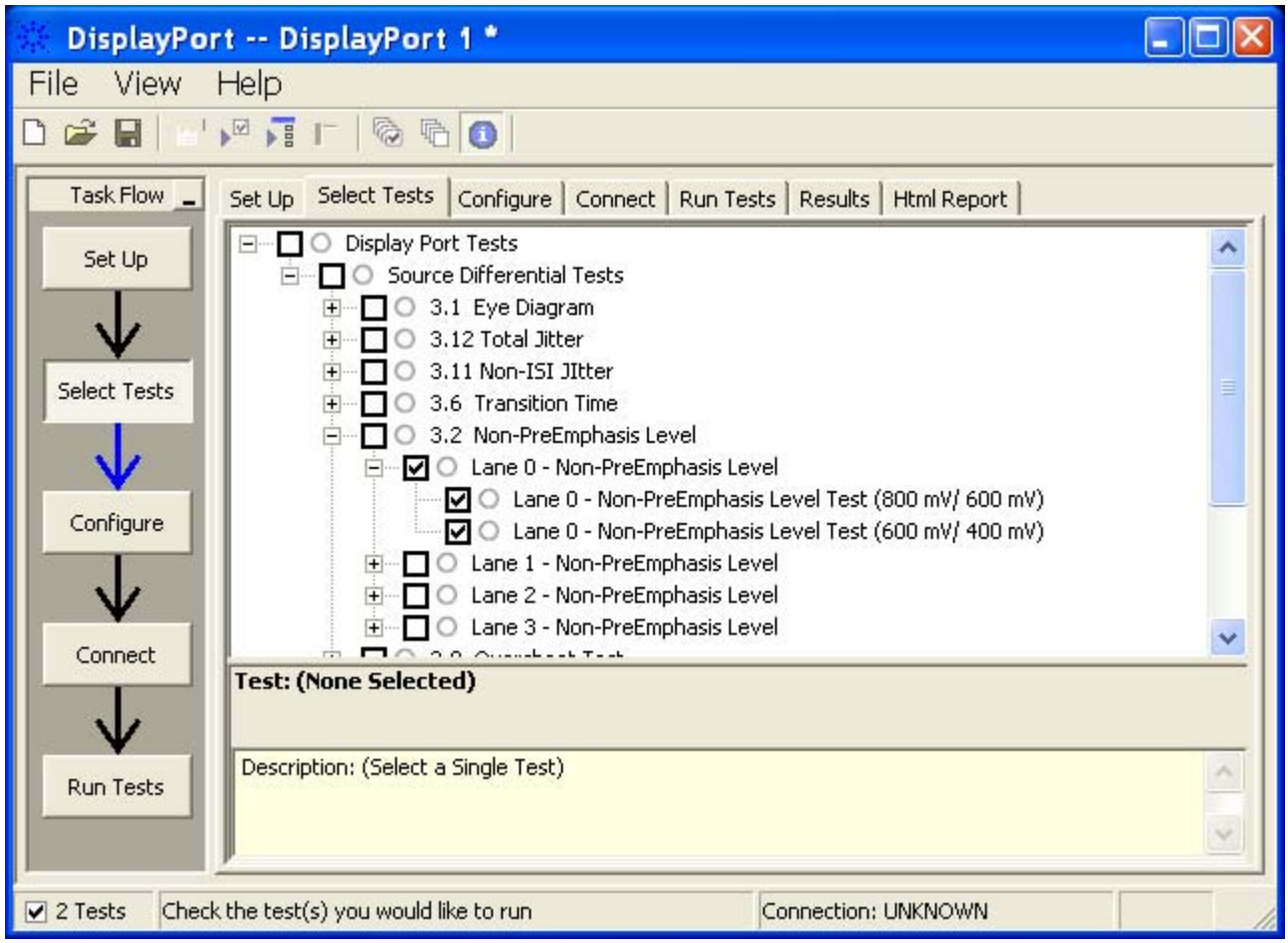

Figure 25 Selecting Non Pre-Emphasis Level Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 12), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 12 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Non Pre-Emphasis	
Level Edges	Sets the number of edges measured for the level test.

Test Condition

Bit Rate: all bit rates are supported (for CTS 1.1a and below), or 5.4Gbps (for CTS 1.2)

Output Level: all output levels are supported.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7 (for RBR and HBR), or 80 Bit Custom Pattern (1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000) (for HBR2).

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

For each level setting testes, the following equation should be used:

Resultant = 20 * Log10[VoltagePeak-Peak_Level A / VoltagePeak-Peak_Level B]

Table 13 Compared Levels

Measurement	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
Reduced-bit Rate (1.62 Gb/s per lane) and High-bit Rate (2.7 Gb/s per lane)		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
High-bit Rate 2 (5.4 Gb/s per lane)		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1.0 dB ≤ Resultant ≤ 4.4 dB

Test References

See Test 3-2: Non Pre-Emphasis Level Verification Testing, in the *DisplayPort- Compliance Test Specification Version 1.2*.

9 Source Overshoot Differential Tests (Informative)

This section provides the guidelines for source overshoot differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Overshoot Differential Tests

When performing the overshoot test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 26 and Figure 27 below show the differential and the single-ended connections for Overshoot Differential Tests.

.

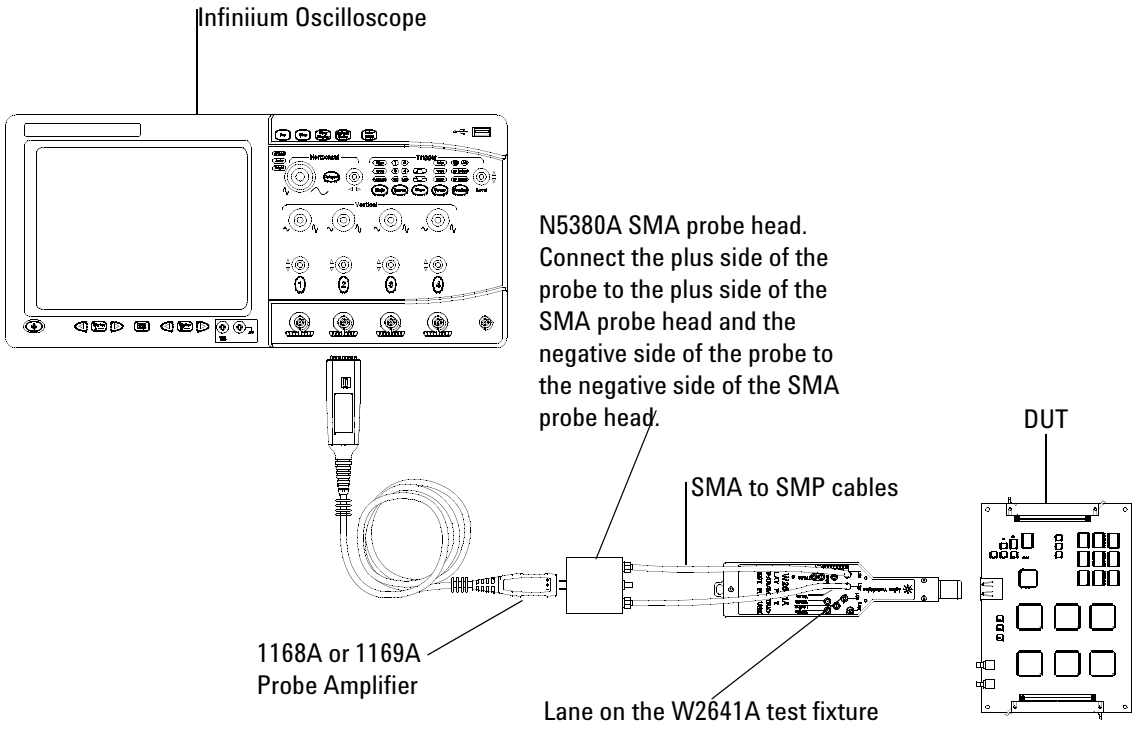

Figure 26 Probing for Differential Tests - Overshoot Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

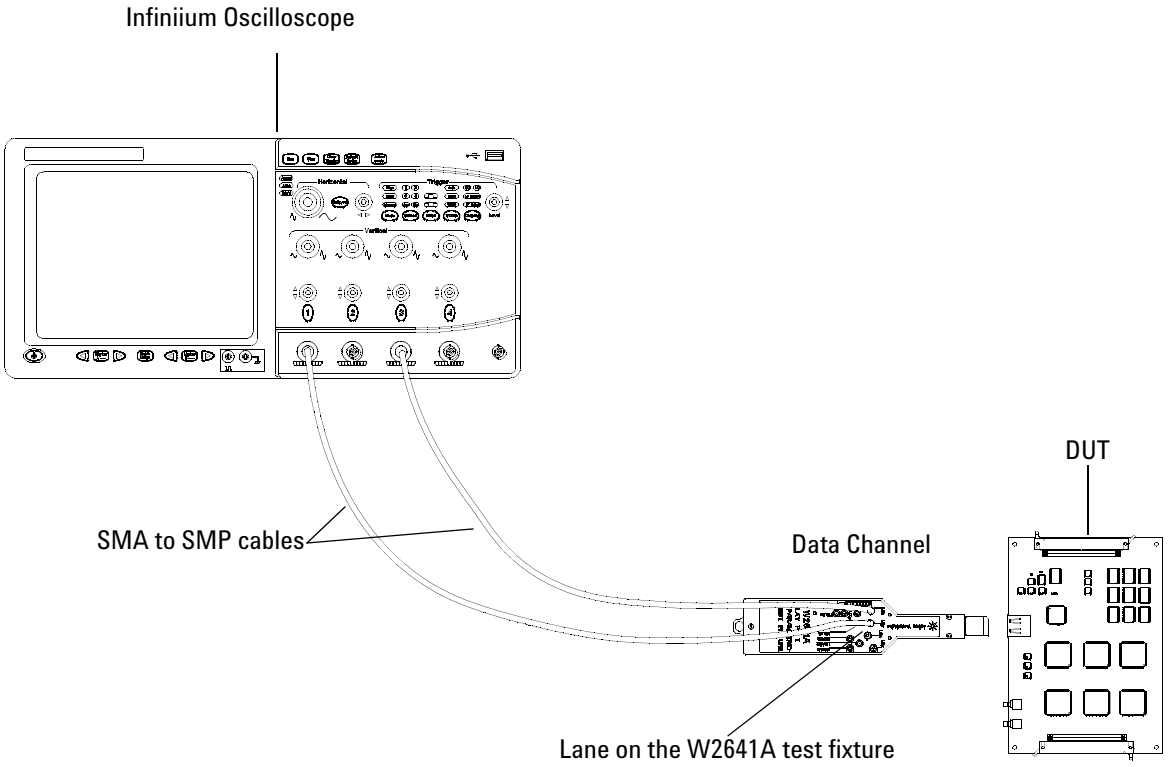

Figure 27 Differential Measurement Setup Using Two Single Ended Connections - Overshoot Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Overshoot Differential Tests

Overshoot is a differential measurement across the outputs of a differential pair. The overshoot test should be performed at the lowest pixel rate.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.
8. This is an Informative test, therefore, the Show Normative Tests Only checkbox must be un-checked.

Navigate to the Overshoot Test - Lane # - Overshoot Test where # is the lane number to be tested.

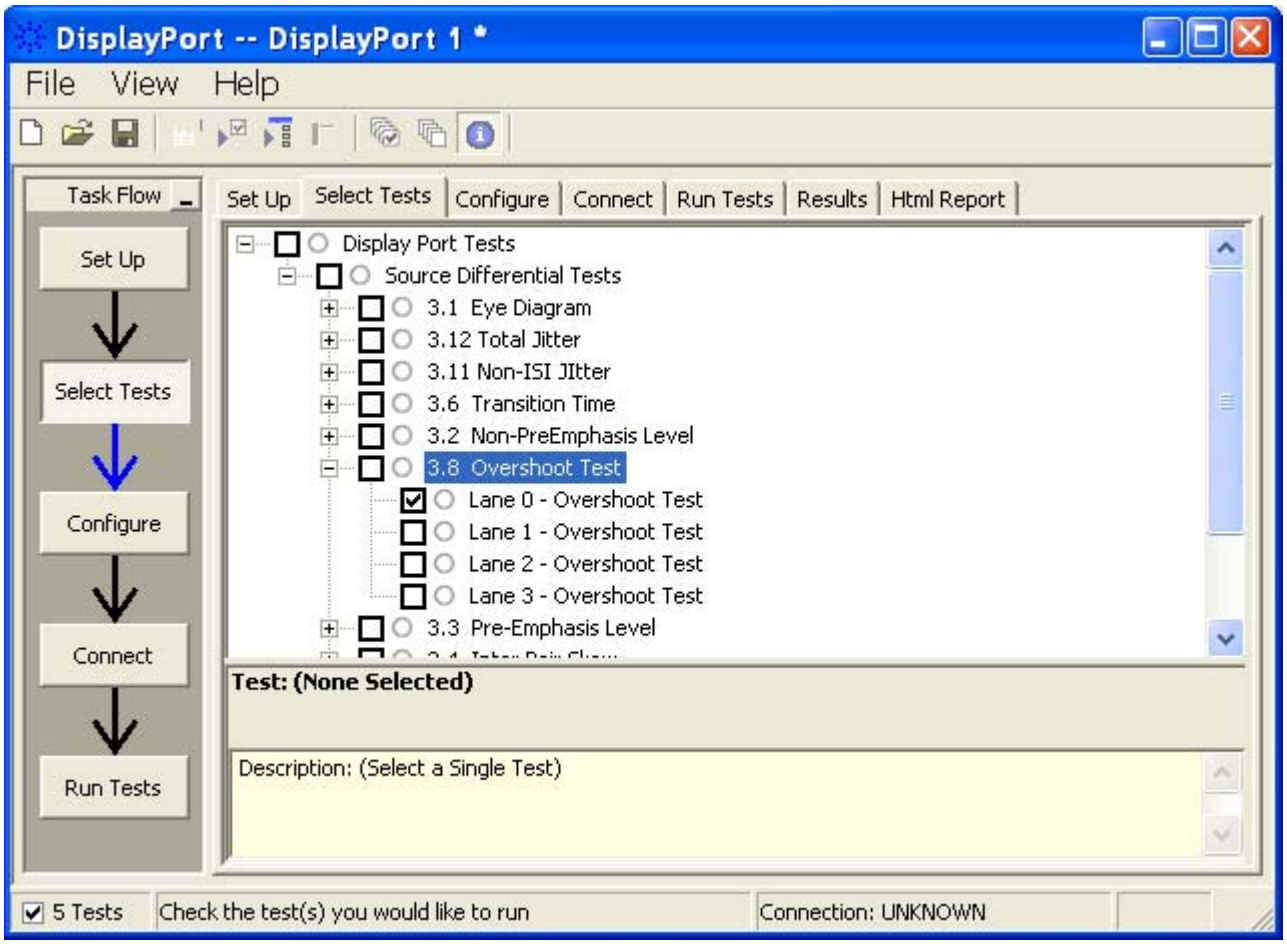

Figure 28 Selecting Overshoot Differential Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 14), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 14 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Overshoot ≤ 25% of the differential swing.

Test References

See section 3.8, in the *DisplayPort- Compliance Test Specification Version 1.1*.

9 Source Overshoot Differential Tests (Informative)

10 Source Pre-Emphasis Level Differential Tests (Normative & Informative)

This section provides the guidelines for source pre-Emphasis level differential tests using an Agilent Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application. In this source test, the Pre-Emphasis Level tests are normative tests whereas Non-Transition Voltage Range Measurements are informative tests.

Probing for Source Pre-Emphasis Level Differential Tests

When performing the pre-Emphasis level differential test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 29 and Figure 30 below show the differential and the single-ended connections for Pre-Emphasis Level Differential Tests.

.

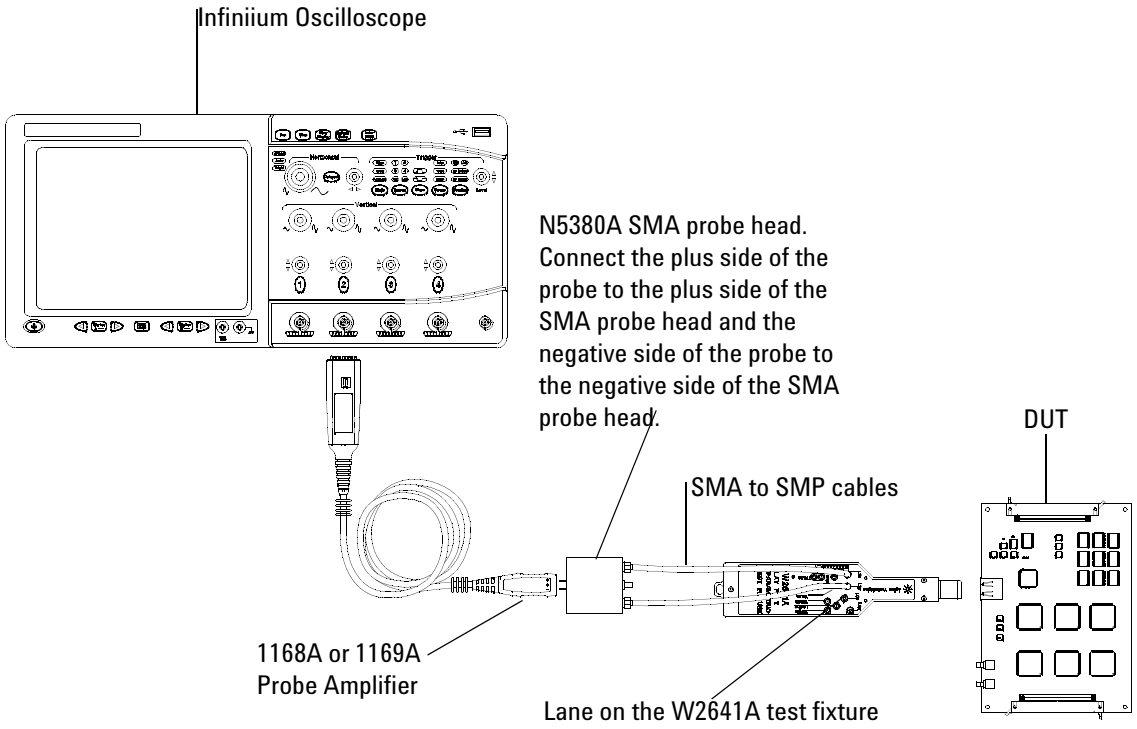

Figure 29 Probing for Differential Tests - Pre-Emphasis Level Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

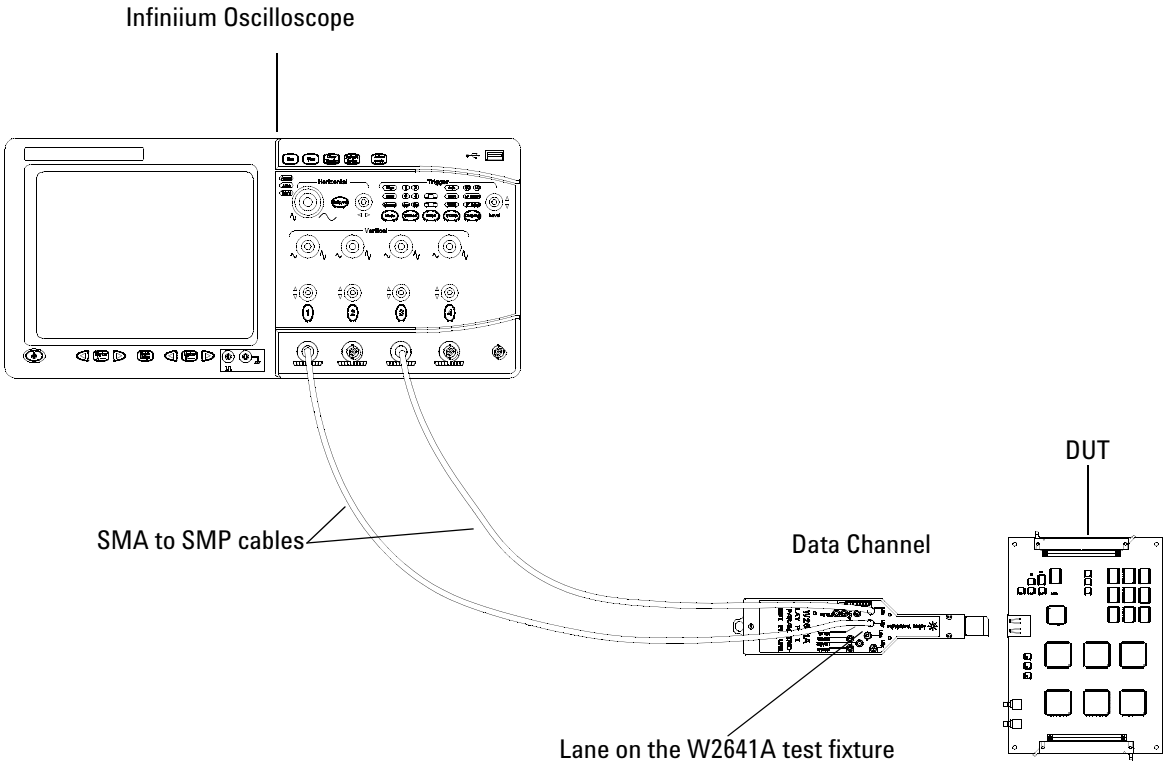

Figure 30 Differential Measurement Setup Using Two Single Ended Connections - Pre-Emphasis Level Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Pre-Emphasis Level Differential Tests

This test evaluates the effect of pre-Emphasis on the source waveform by measuring the peak differential amplitude and assuring the accuracy of the pre-Emphasis setting. (Reference: Table 3.10 VESA DisplayPort Standard).

The source can apply pre-Emphasis to the waveform in order to overcome the harmful effects caused by such things as system losses through pc boards, connectors, and cables. The standard stipulates the relative magnitude to overcome specific losses. Because pre-Emphasis is negotiated, two units with substantially different degrees of pre-Emphasis may be seen as non-interoperable under certain conditions. This test ensures that the system loss or pre-Emphasis budget is obeyed.

For Compliance Test Specifications 1.1a and below, tests must be made on all bit rates supported with pre-Emphasis for all differential voltage swings supported using a test pattern of PRBS 7. For Compliance Test Specifications 1.2, tests must be made on a bit rate of 5.4Gbps using an 80 bit custom pattern (1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000).

The following equation is used to calculate the pre-Emphasis result:

$$\text{Pre-emphasis Result} = 20\log\left(\frac{V_{Swingpe}}{V_{Swingnope}}\right)$$

$$V_{Swingpe} = (V_{Hpe} - V_{Lpe})$$

$$V_{Swingnope} = (V_{Hnope} - V_{Lnope})$$

where:

V_{Hpe} = the high voltage value is measured using the histogram modes at the top for transition eyes.

V_{Lpe} = the low voltage value is measured using the histogram modes at the top for transition eyes.

V_{Hnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

V_{Lnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.
8. The Non-Transition Voltage Range Measurement test is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

Navigate to the Pre-Emphasis Level - Lane # - Pre-Emphasis Level Test or Lane # - Non-Transition Voltage Range Measurement where # is the lane number to be tested.

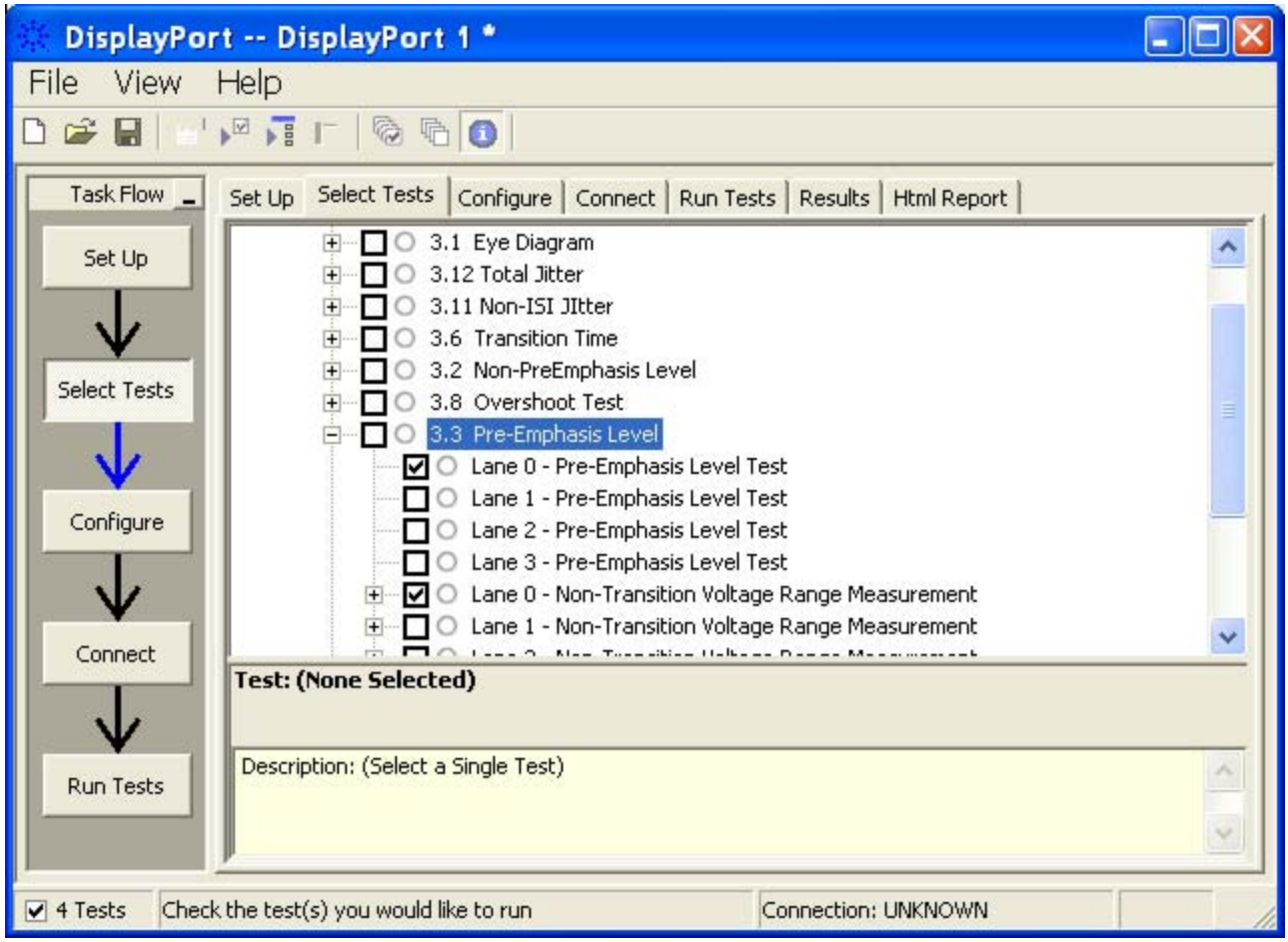

Figure 31 Selecting Pre-Emphasis Level Differential Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 15), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 15 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	

Table 15 Test Configuration Options

Configuration Option	Description
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
PreEmphasis Level	
PreEmphasis Edge	Sets the number of edges measured for the Pre-Emphasis Level test.

Test Condition

Bit Rate: all bit rates are supported (for CTS 1.1a and below), or 5.4Gbps (for CTS 1.2).

Output Level: all output levels are supported.

Pre-Emphasis: all the pre-Emphasis supported settings are subject to the constraints listed in Table 3-12 of the DisplayPort Standard.

Test Pattern: PRBS 7 (for RBR and HBR), or 80 Bit Custom Pattern (1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000 1111100000) (for HBR2).

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

The pre-Emphasis calculation must fall within the following ranges for each pre-Emphasis level (CTS 1.1a):

0 dB setting: 0.25 dB $\geq$ Resultant $\geq$ -8.4 dB

3.5 dB setting: Resultant3.5dB $\geq$ 2.0 dB

6.0 dB setting: Resultant6.0dB $\geq$ Resultant3.5dB + 1.6

9.5 dB setting: Resultant9.5dB $\geq$ Resultant6.0dB + 1.6

The non-transition voltage range measurement calculation must fall within the following ranges (CTS 1.1a):

Resultant < 0.7

The pre-Emphasis calculation must fall within the following ranges for each pre-Emphasis level (CTS 1.2):

Level 0 - OFF Pre-Emphasis Measurement

+.25 dB - Resultant

Level 0, Level 1, Level 2, and Level 3 Ratio Measurements

For Level 1 vs. Level 0 Pre-emphasis settings: $Resultant_{Lvl0\ to\ Lvl1} \geq 2.0$ dB

For Level 2 vs. Level 1 Pre-emphasis settings: $Resultant_{Lvl1\ to\_Lvl2} \geq 1.6$ dB

For Level 3 vs. Level 2 Pre-emphasis settings: $Resultant_{Lvl2\_to\_Lvl3} \geq 1.6$ dB

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant >0.708 OR 20*log(Resultant) >-3dB

For Level 1 voltage setting: Resultant >0.708 OR 20*log(Resultant) >-3dB

For Level 0 voltage setting: Resultant >0.85 OR 20*log(Resultant) >-1.4dB

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.2 draft8* and Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1a*.

11 Source PostCursor 2 Verification Tests (Normative)

This section provides the guidelines for source postCursor 2 verification tests using an Agilent Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source PostCursor 2 Verification Tests

When performing the postCursor2 verification test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 32 and Figure 33 below show the differential and the single-ended connections for PostCursor 2 Verification Tests.

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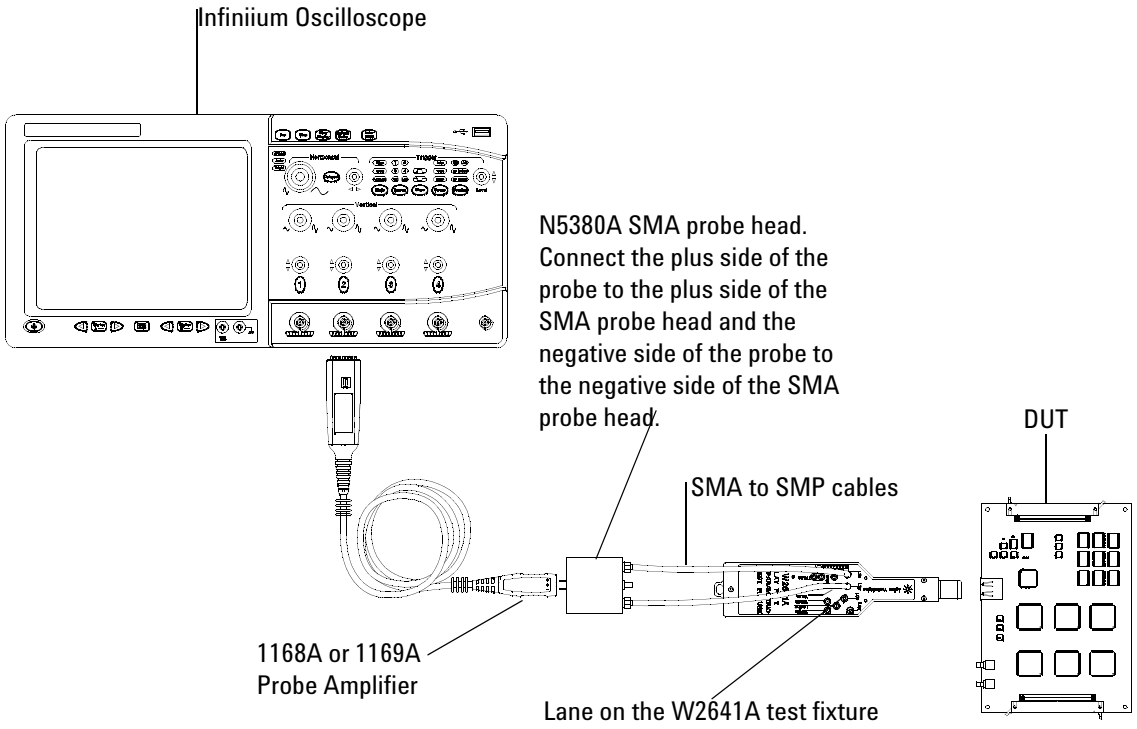

Figure 32 Probing for Differential Tests - PostCursor 2 Verification Tests (Single Connection with W2641A DisplayPort Test Fixture)

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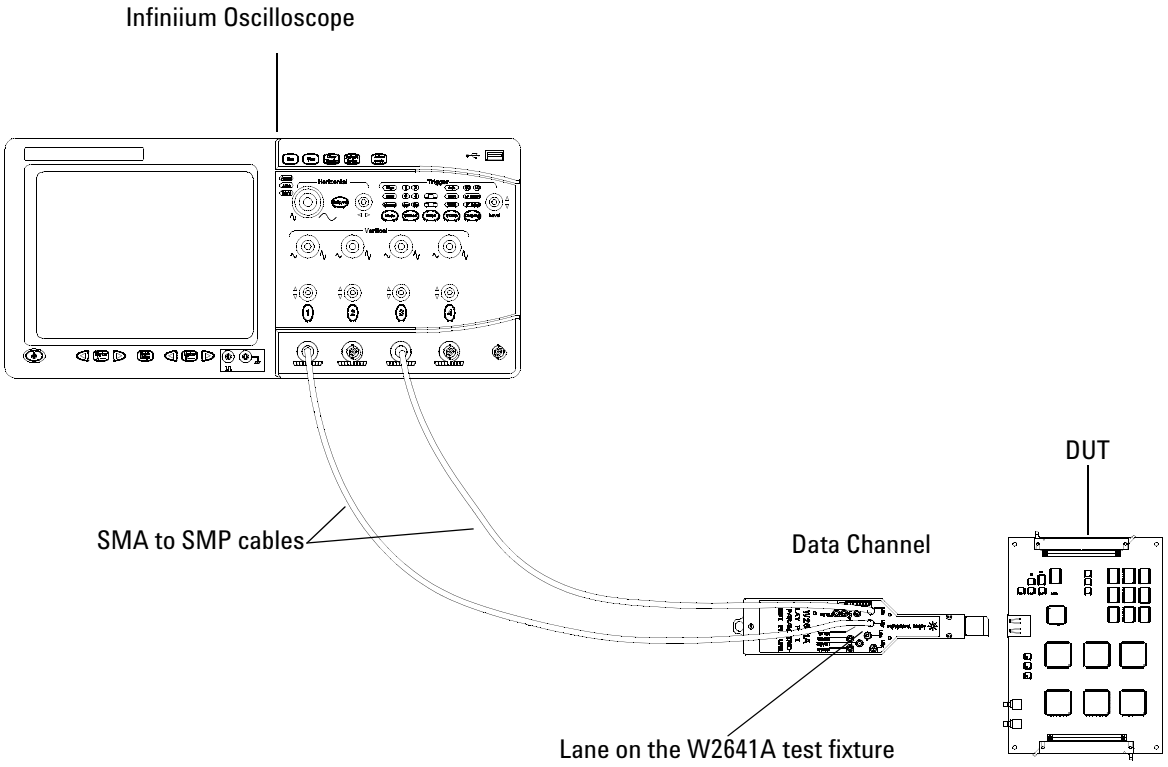

Figure 33 Differential Measurement Setup Using Two Single Ended Connections - PostCursor 2 Verification Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source PostCursor 2 Verification Tests

This test evaluates the effect of adding PostCursor 2 in a source waveform by measuring the peak differential amplitude to assure accuracy of the PostCursor 2 setting. (Reference: Table 3-2 VESA DisplayPort Standard 1.2).

For all data rates, in addition to pre-emphasis levels, the source is given the capability to provide three pre-emphasis PostCursor 2 levels. Pre-emphasis and PostCursor 2 are used in conjunction to optimize the main link waveform to overcome system losses, such as through PC boards, connectors, and cables. The standard stipulates the relative magnitude to overcome specific losses. Because pre-emphasis and PostCursor 2 will be negotiated, two units with substantially different degrees of pre-emphasis and PostCursor 2 levels can be interoperable by operating at different settings. This test ensures that control of PostCursor 2 settings has the desired affect on improving signal quality in the link.

Tests must be made on a bit rate of 5.4Gbps using an 80 bit custom pattern defined as follows:

- 3x (5 ones, 5 zeros), 8x (1100), 9x (10)

1111100000 1111100000 1111100000 1100110011 0011001100 1100110011 0010101010 1010101010

For each voltage swing and pre-emphasis level, transition bit voltages are measured at qualified sections of the pattern. Each transition swing is composed of High and Low voltage measurements which are combined to obtain the peak-to-peak voltage.

For PostCursor 2 Levels 0, 1, 2, 3:

$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_\ PC2\_LvlX\_L}$;

where X corresponds to the PostCursor 2 Level 0, 1, 2, or 3.

$V_{T1010\_PC2\_LvlX}$ measurements are defined as the average value over the 40% to 70% UI points in the fifth transition bit in the 1010 portion of the pattern. V_{T1010_H} measurements are made on the isolated ‘1’ portion of the waveform, and V_{T1010_L} measurements are made on the isolated ‘0’ portion of the waveform.

$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_LvlX\_H} - V_{T1100\_LvlX\_L}$;

where X corresponds to the PostCursor 2 Level 0, 1, 2, or 3.

$V_{T1100\_PC2\_LvlX}$ measurements are defined as the average value over the 40% to 70% UI points in the fifth transition bit in the 1100 portion of the pattern. V_{T1100_H} measurements are made on the ‘11’ portion of the waveform, and V_{T1100_L} measurements are made on the ‘00’ portion of the waveform.

Level X: Resultant = [$V_{T1100\_PC2\_LvlX\_PP}$ / $V_{T1010\_PC2\_LvlX\_PP}$] for all voltage swing and pre-emphasis level combinations.

Test Procedure

1. Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to “3.3 Post Cursor2 Verification Tests”.

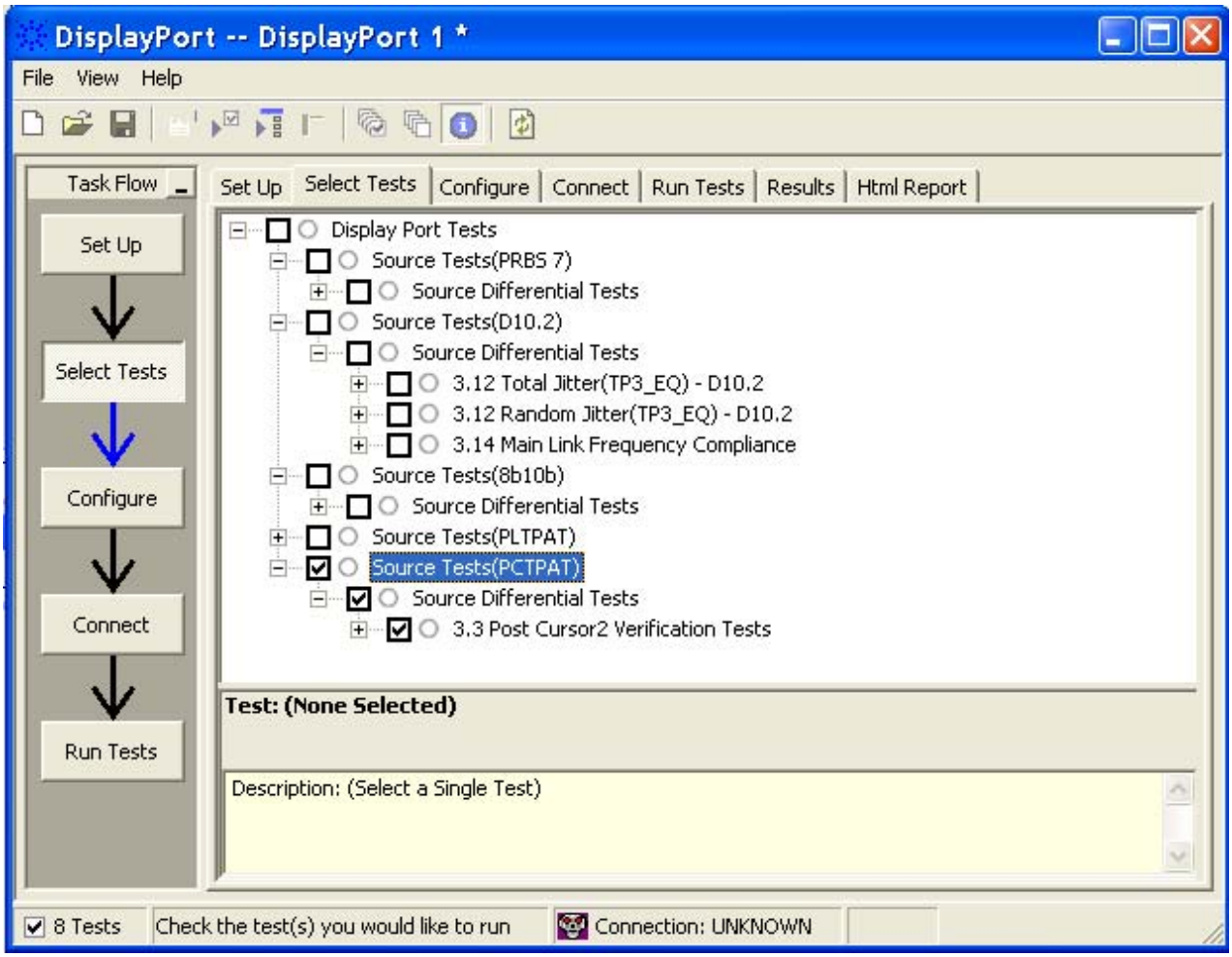

Figure 34 Selecting PostCursor 2 Verification Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options (see Table 16), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 16 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition

Table 16 Test Configuration Options

Configuration Option	Description
	Source Differential Tests
PostCursor 2 Verification Tests	
PostCursor 2 Edges	Sets the number of edges measured for the PostCursor 2 verification test.

Test Condition

Bit Rate: 5.4Gbps.

Output Level: all output levels are supported.

Pre-Emphasis: all Pre-Emphasis Levels supported are subject to the constraints in Table 3-1 of the VESA DisplayPort1.2 Standard.

Test Pattern: 80 Bit Custom Pattern defined as follows:

- 3x (5 ones, 5 zeros), 8x (1100), 9x (10)

1111100000 1111100000 1111100000 1100110011 0011001100 1100110011 0010101010 1010101010.

PostCursor 2 Level: all PostCursor 2 levels are supported.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

The PostCursor 2 measurements are calculated using the following equations:

Level 1 vs. Level 0: Resultant = 20*Log [Resultant_{Lvl1} / Resultant_{Lvl0}] for all output level and pre-emphasis level combinations supported.

Level 2 vs. Level 1: Resultant = 20*Log [Resultant_{Lvl2} / Resultant_{Lvl1}], for all output level and pre-emphasis level combinations supported.

Level 3 vs. Level 2: Resultant = 20*Log [Resultant_{Lvl3} / Resultant_{Lvl2}], for all output level and pre-emphasis level combinations supported.

The resultant specifications are defined as follows:

Level 1 vs. Level 0 pre-emphasis settings: $\text{Resultant}_{Lvl0\_to\_Lvl1} \leq -0.45\text{dB}$

Level 2 vs. Level 1 pre-emphasis settings: $\text{Resultant}_{Lvl1\_to\_Lvl2} \leq -0.5\text{dB}$

Level 3 vs. Level 2 pre-emphasis settings: $\text{Resultant}_{Lvl2\_to\_Lvl3} \leq -0.6\text{dB}$

Test References

See Test 3.3.2: PostCursor 2 Verification Testing, in the *DisplayPort- Compliance Test Specification Version 1.2*.

11 Source PostCursor 2 Verification Tests (Normative)

12 Source Inter Pair Skew Differential Tests

This section provides the guidelines for source inter pair skew differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Inter Pair Skew Differential Tests

When performing the inter pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 35 and Figure 36 below show the differential and the single-ended connections for Inter Pair Skew Differential Tests..

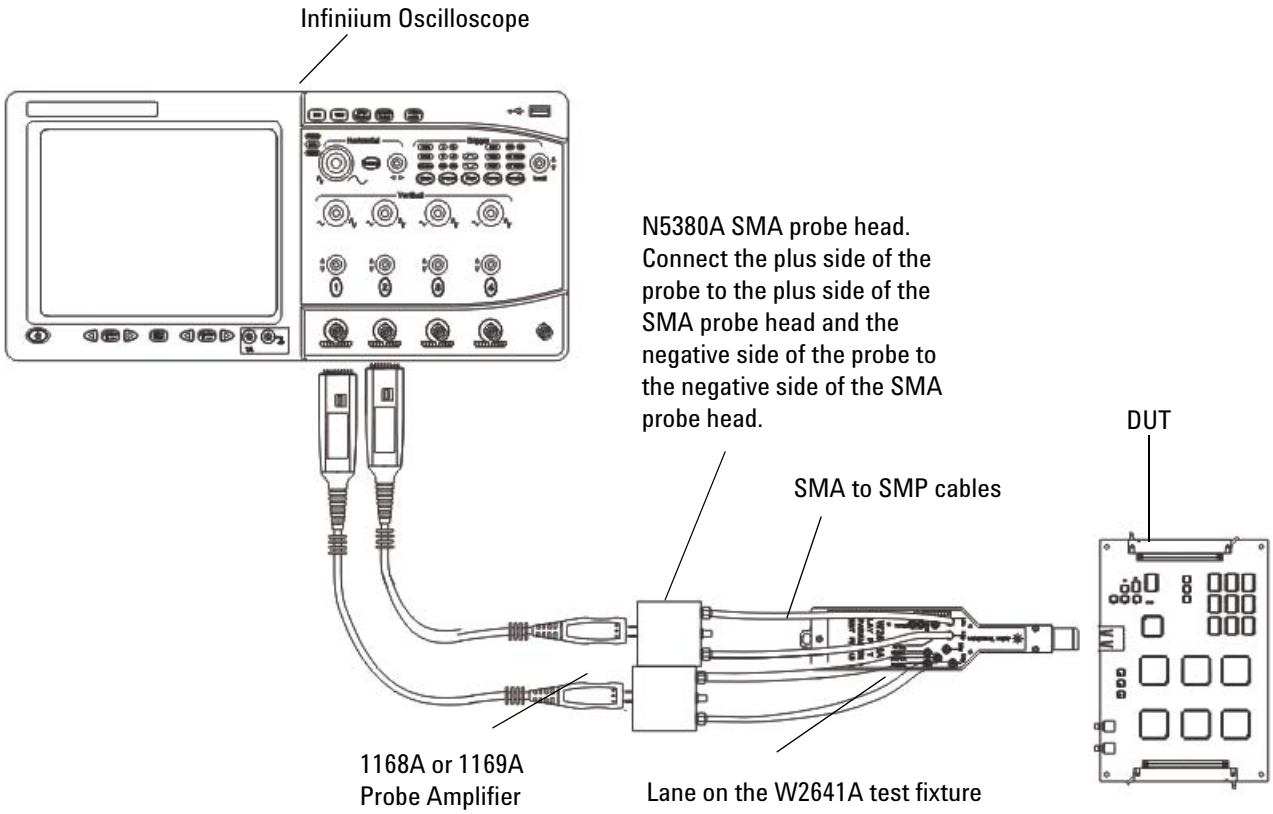

Figure 35 Probing for Differential Tests - Inter Pair Skew Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

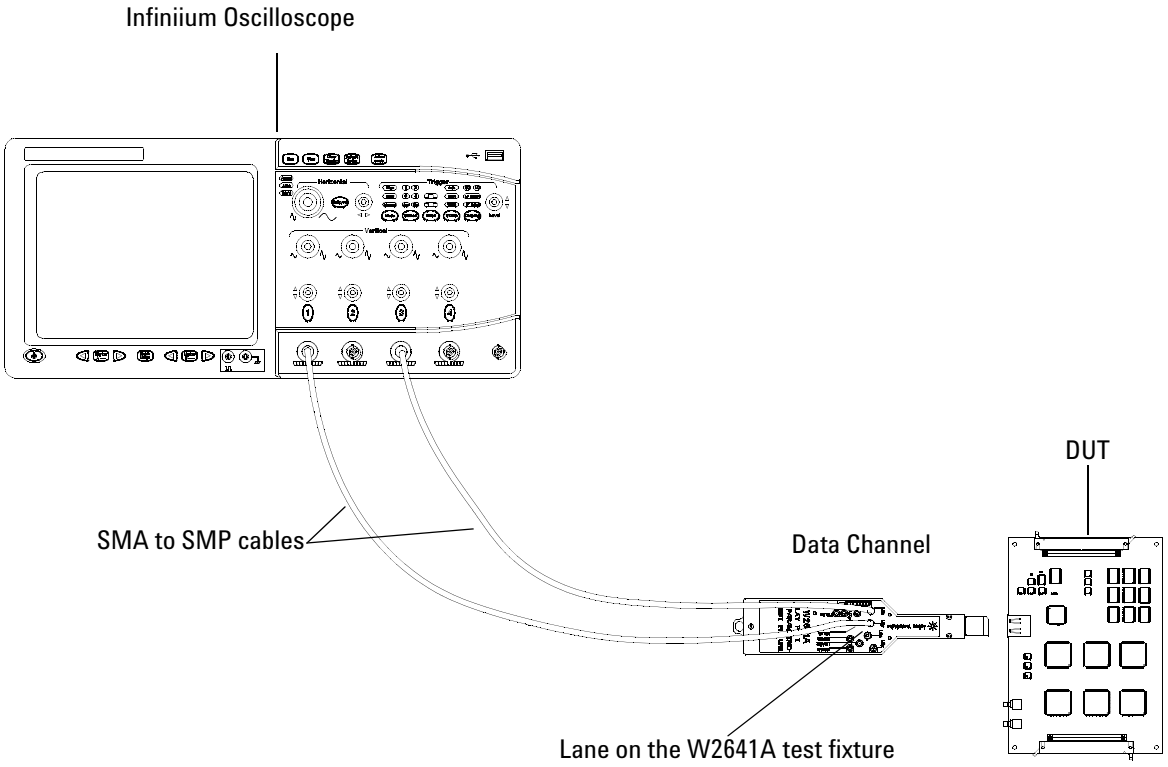

Figure 36 Differential Measurement Setup Using Two Single Ended Connections - Inter Pair Skew Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Inter Pair Skew Differential Test

The inter pair skew test evaluates the skew, or time delay, between respective differential data lanes in the DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard).

The DisplayPort interface has the ability to skew, or deskew lanes by 20 UI (Unit Intervals) which is as much as 12ns (1.62Gb/s) and is intended to eliminate simultaneous degradation of concurrent bytes of transmitted data. The specification at 150 ps at the package pins (TP1), likely to be degraded another 50 ps through the connector, is less than 0.5 UI at the highest bit rate. Therefore, it is unlikely to be a significant reason for non-interoperability.

Channel-to-channel de-skew must be performed on the two oscilloscope channels used for this measurement (see “Differential Probe Head Skew Calibration" on page 291 and “SMA Probe Head Skew Calibration" on page 297).

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Inter Pair Skew - Lane # - Inter Pair Skew Test where # is the lane number to be tested.

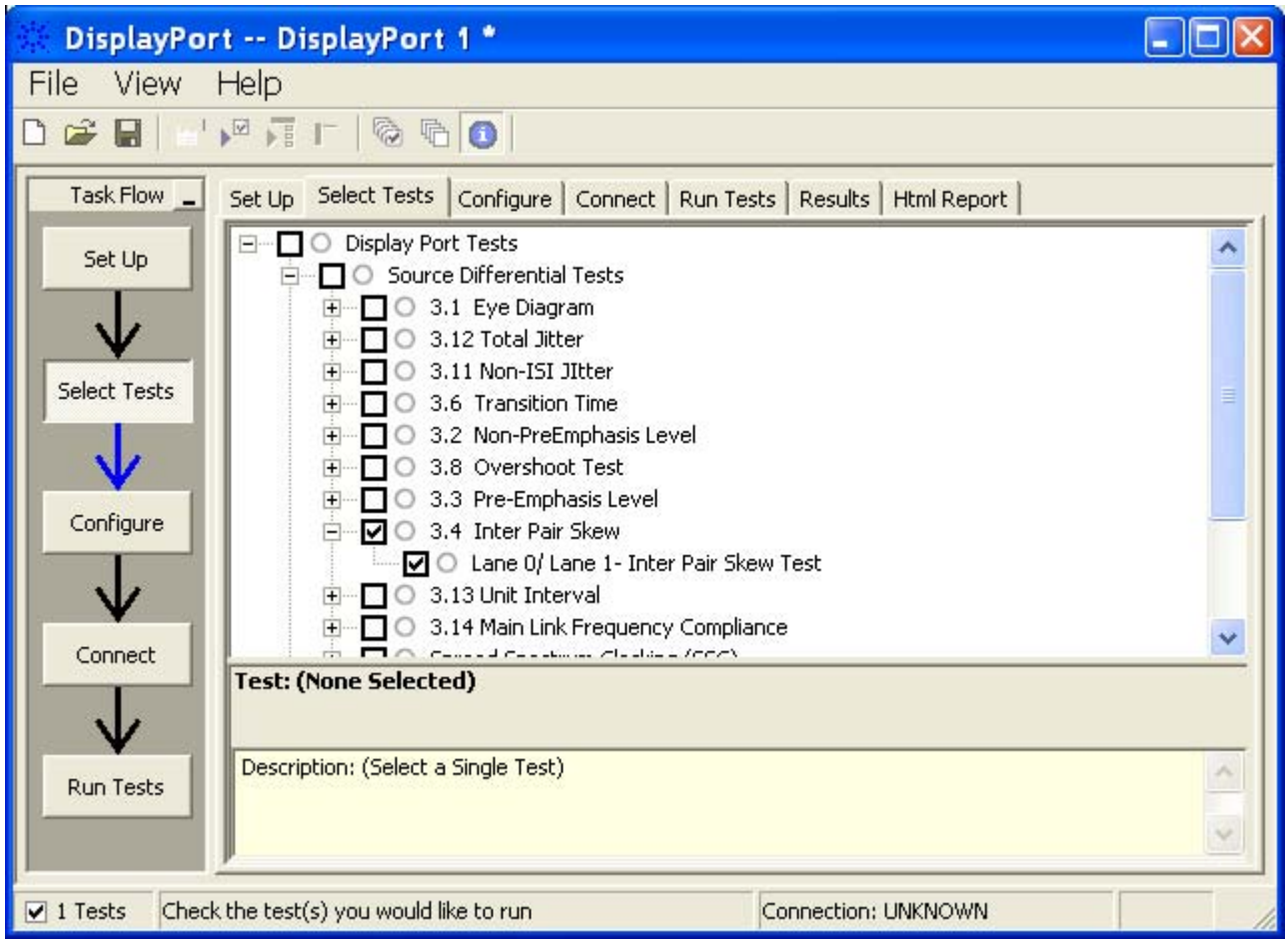

Figure 37 Selecting Inter Pair Skew Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 17), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 17 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Inter Pair Skew	
Inter Pair Skew Edges	Sets the number of edges measured for the inter pair skew test.

Table 17 Test Configuration Options

Configuration Option	Description
Maximum Retries	Sets the number of re-tries for the inter pair skew test.
Trigger Patterns	Define trigger pattern other than the default pattern.

Test Condition

Bit Rate: highest bit rate is supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

CTS 1.1a: -2 UI ≤ Inter Pair Skew ≤ 2 UI

CTS 1.2:

- If the highest bit rate is RBR or HBR: -2 UI ≤ Inter Pair Skew ≤ 2 UI
- If the highest bit rate is HBR2: -(4 UI + 500 ps) ≤ Inter Pair Skew ≤ (4UI + 500 ps)

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.2 draft8* and Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1a.*

12 Source Inter Pair Skew Differential Tests

13 Source Unit Interval Differential Tests (Informative)

This section provides the guidelines for source unit interval differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Unit Interval Differential Tests

When performing the unit interval test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 38 and Figure 39 below show the differential and the single-ended connections for Unit Interval Differential Tests.

.

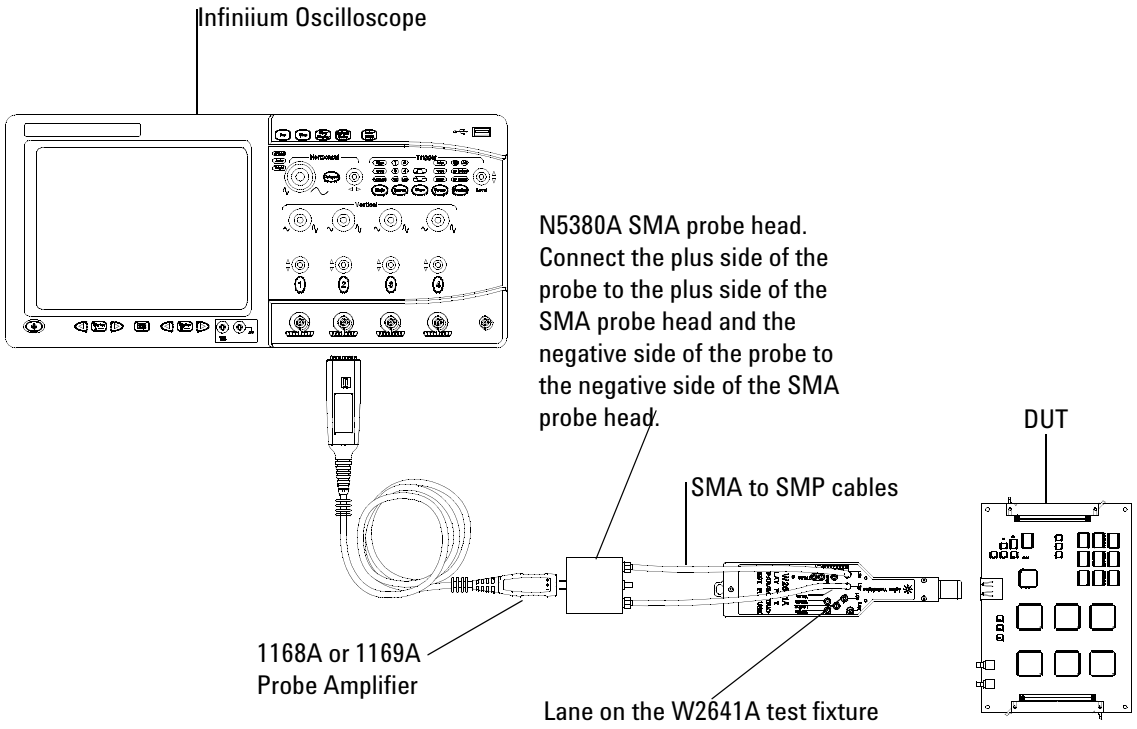

Figure 38 Probing for Differential Tests - Unit Interval Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

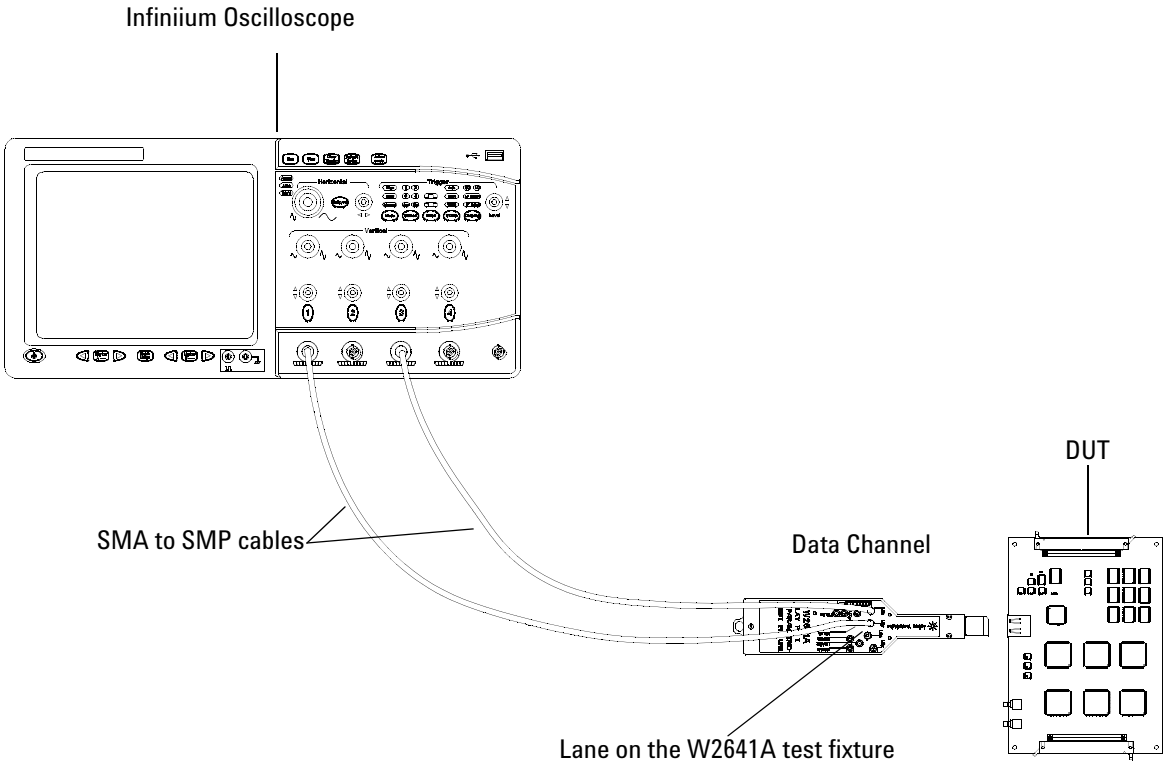

Figure 39 Differential Measurement Setup Using Two Single Ended Connections - Unit Interval Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Unit Interval Differential Tests

Unit interval test evaluates the overall variation in the UI width over at least one full typical SSC cycle to ensure it stays within the specification limit.

This test calculates the average unit interval with and without the spread spectrum clocking which will have very little to do with interoperability unless the unit interval is at the extremes.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.
8. This is an Informative test, therefore, the Show Normative Tests Only checkbox must be un-checked.

Navigate to the Unit Interval - Lane # - SSC Unit Interval Test where # is the lane number to be tested.

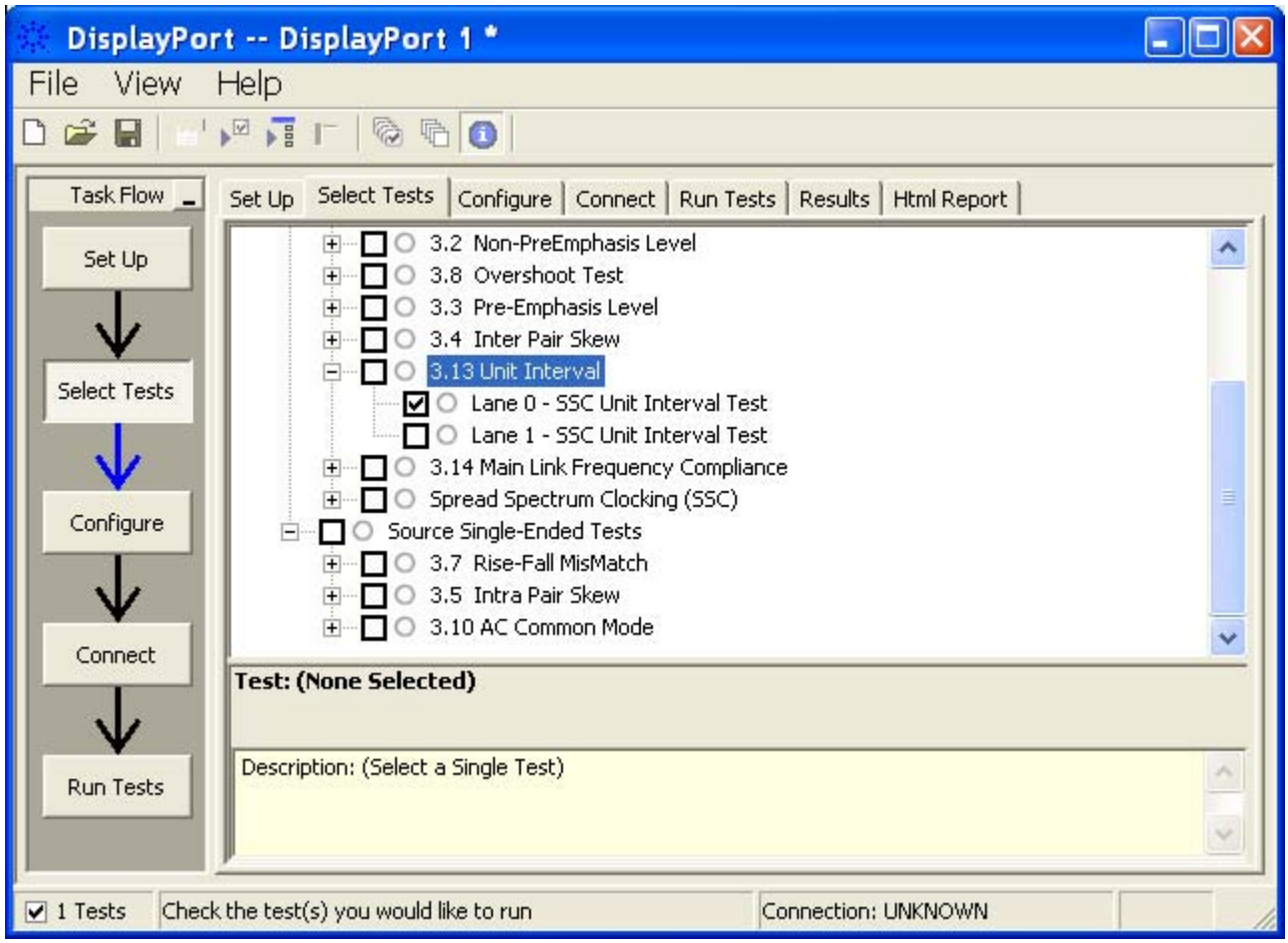

Figure 40 Selecting Unit Interval Differential Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 18), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 18 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

An evaluation of at least 100K Unit Intervals or 1 full SSC cycle is required to ensure that any SSC modulation on the signal does not violate the timebase accuracy specifications.

PASS Condition

For Reduced Bit Rate:

[1/1.62e9]*[1-0.0003] ≤ Mean Unit Interval ≤ [1/1.62e9]*[1+.0053]

For High Bit Rate:

[1/2.7 e9]*[1-0.0003] ≤ Mean Unit Interval ≤ [1/2.7e9]*[1+.0053]

Test References

See section 3.6, in the *DisplayPort- Compliance Test Specification Version 1.1*.

13 Source Unit Interval Differential Tests (Informative)

14 Source Main Link Frequency Compliance Differential Tests

This section provides the guidelines for the source main link frequency compliance tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Main Link Frequency Compliance Differential Tests

When performing the source main link frequency compliance tests, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 41 and Figure 42 below show the differential and the single-ended connections for Main Link Frequency Compliance Tests.

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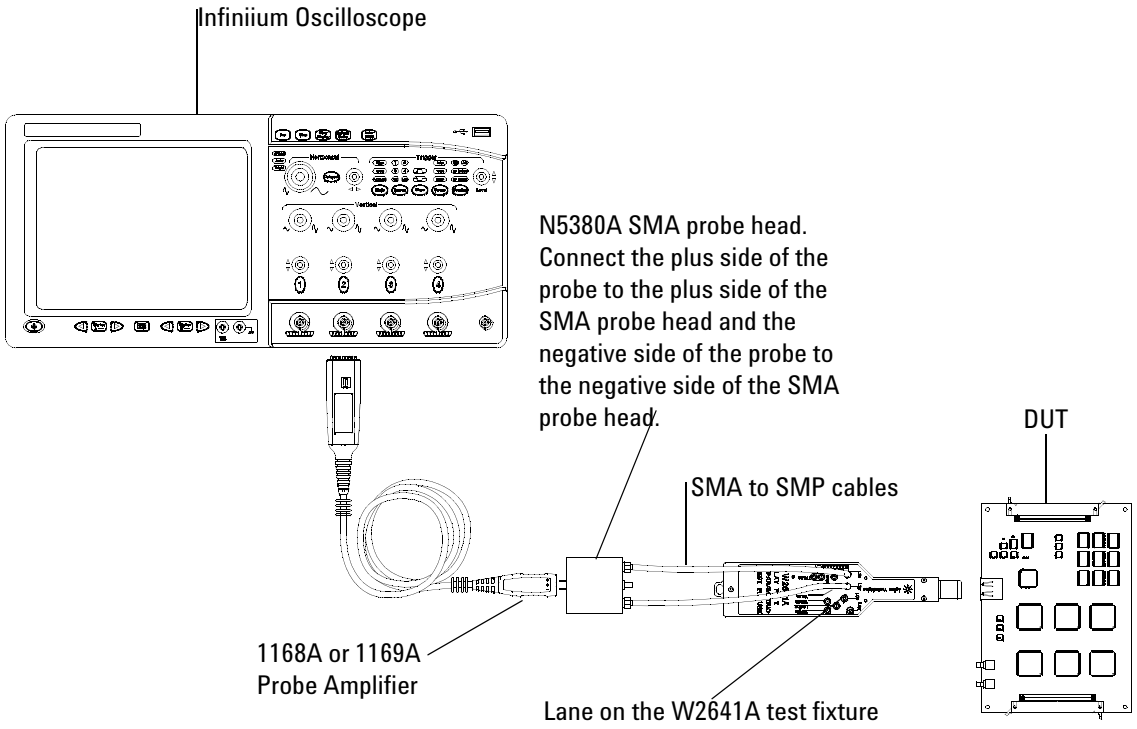

Figure 41 Probing for Differential Tests - Main Link Frequency Compliance Tests (Single Connection with W2641A DisplayPort Test Fixture)

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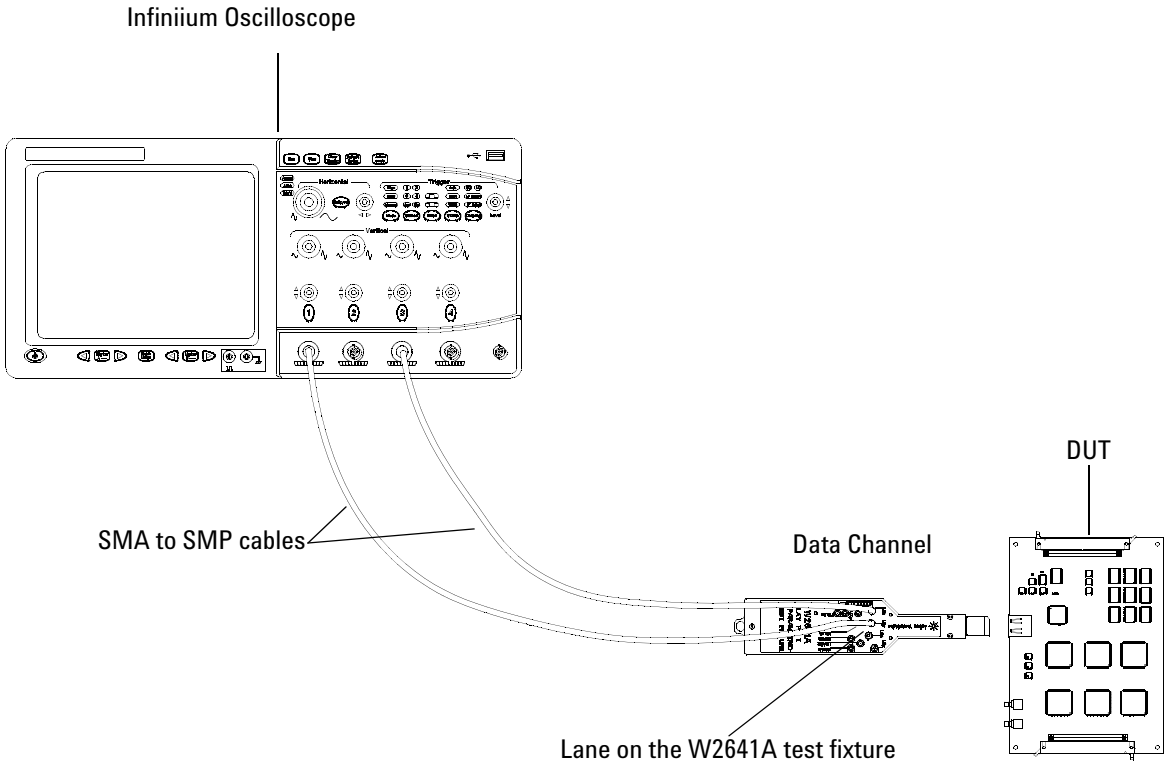

Figure 42 Differential Measurement Setup Using Two Single Ended Connections - Main Link Frequency Compliance Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Main Link Frequency Compliance Differential Tests

The main link frequency compliance test evaluates the overall variation in source time base accuracy, ensuring the device stays within the required +- 300 PPM limit. Tests shall be performed on a PRBS 7 signal with SSC disabled. An evaluation of at least 10 acquisitions is required.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Main Link Frequency Compliance - Lane # - Main Link Frequency Compliance where # is the lane number to be tested.

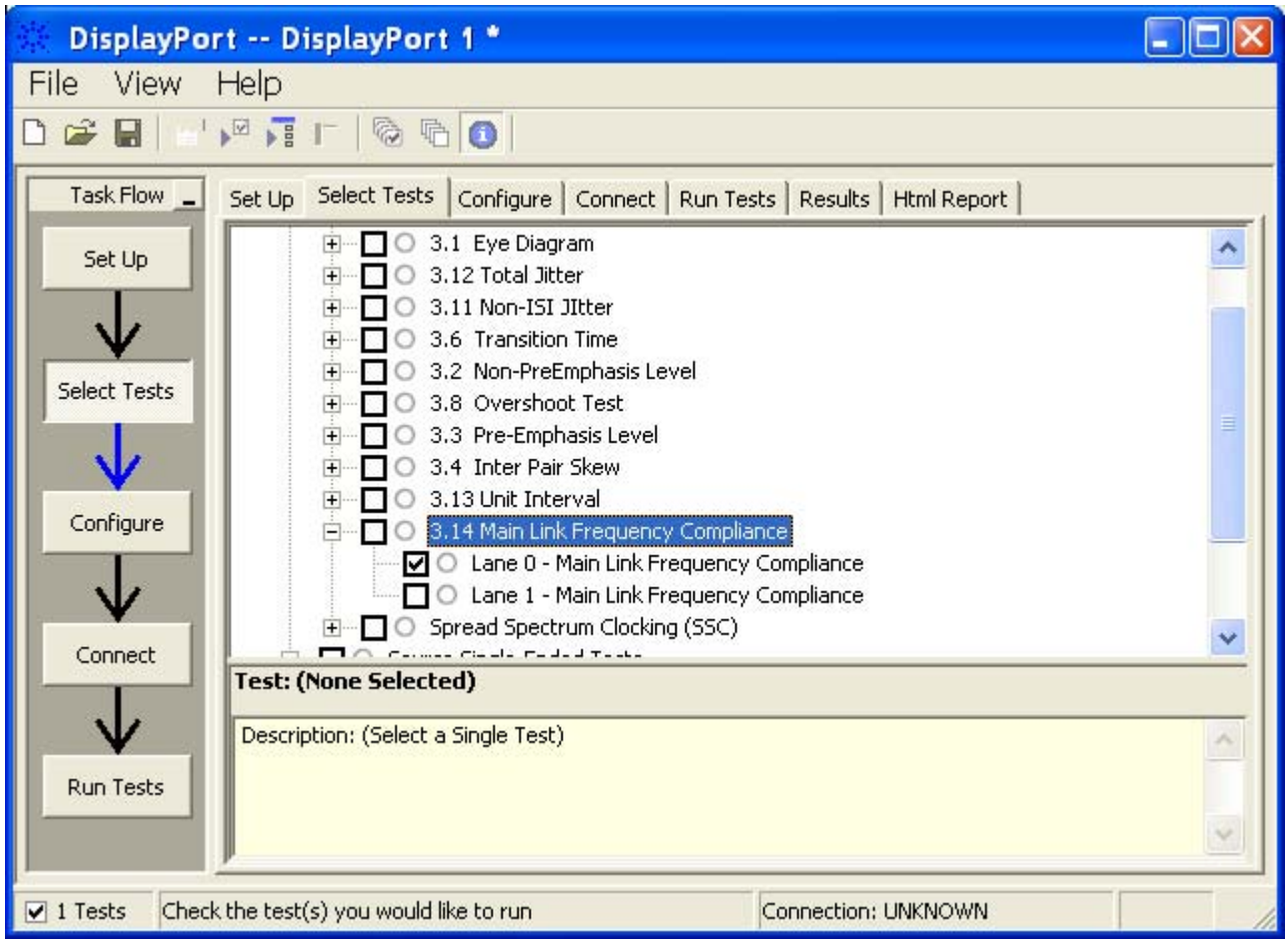

Figure 43 Selecting Main Link Frequency Compliance Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 19), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 19 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

An evaluation of at least 10 full SSC cycles are required.

PASS Condition

The Main Link Frequency Compliance Test result must satisfy the following criteria:

SSC $\text{frequency}_{\text{ppm}} \leq 300$.

Test References

See Test 3.14: Main Link Frequency Compliance Tests, in the *DisplayPort- Compliance Test Specification Version 1.1*.

15 Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)

This section provides the guidelines for the source spread spectrum clocking (SSC) differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application. In this SSC test, the Modulation Frequency and Modulation Deviation tests are normative tests whereas Deviation HF Variation tests are informative tests.

Probing for Source Spread Spectrum Clocking (SSC) Differential Tests

When performing the spread spectrum clocking (SSC) test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 44 and Figure 45 below show the differential and the single-ended connections for Spread Spectrum Clocking (SSC) Differential Tests.

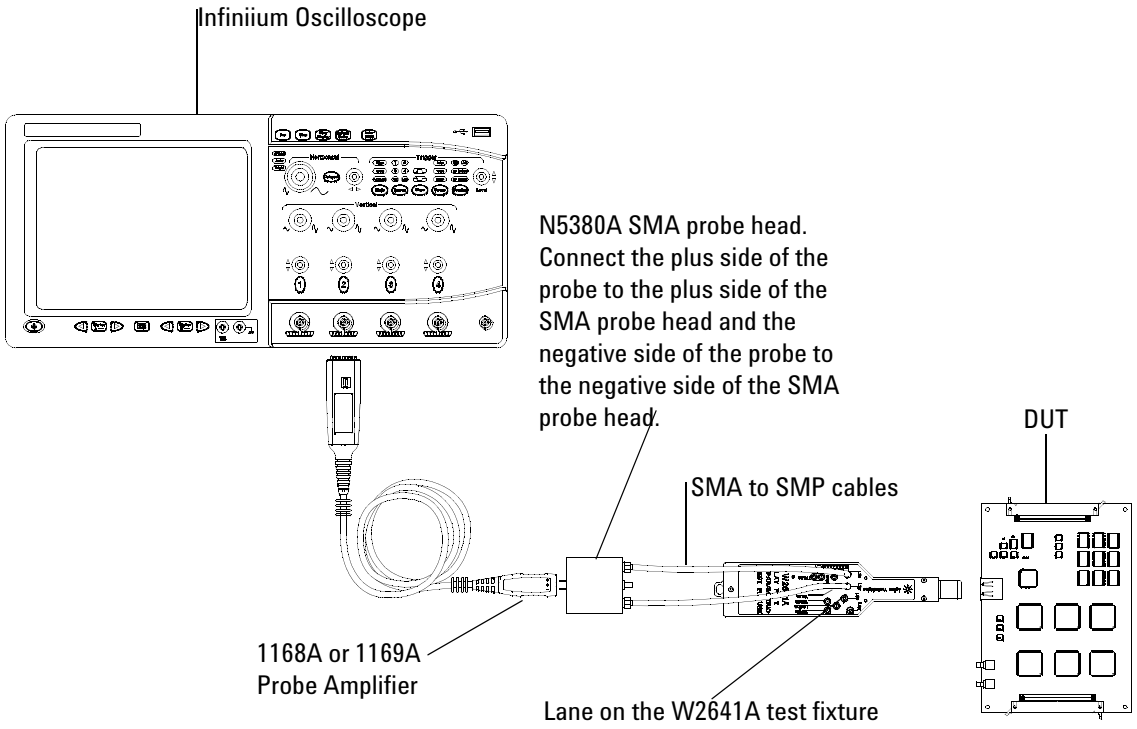

Figure 44 Probing for Differential Tests - SSC Tests (Single Connection with W2641A DisplayPort Test Fixture)

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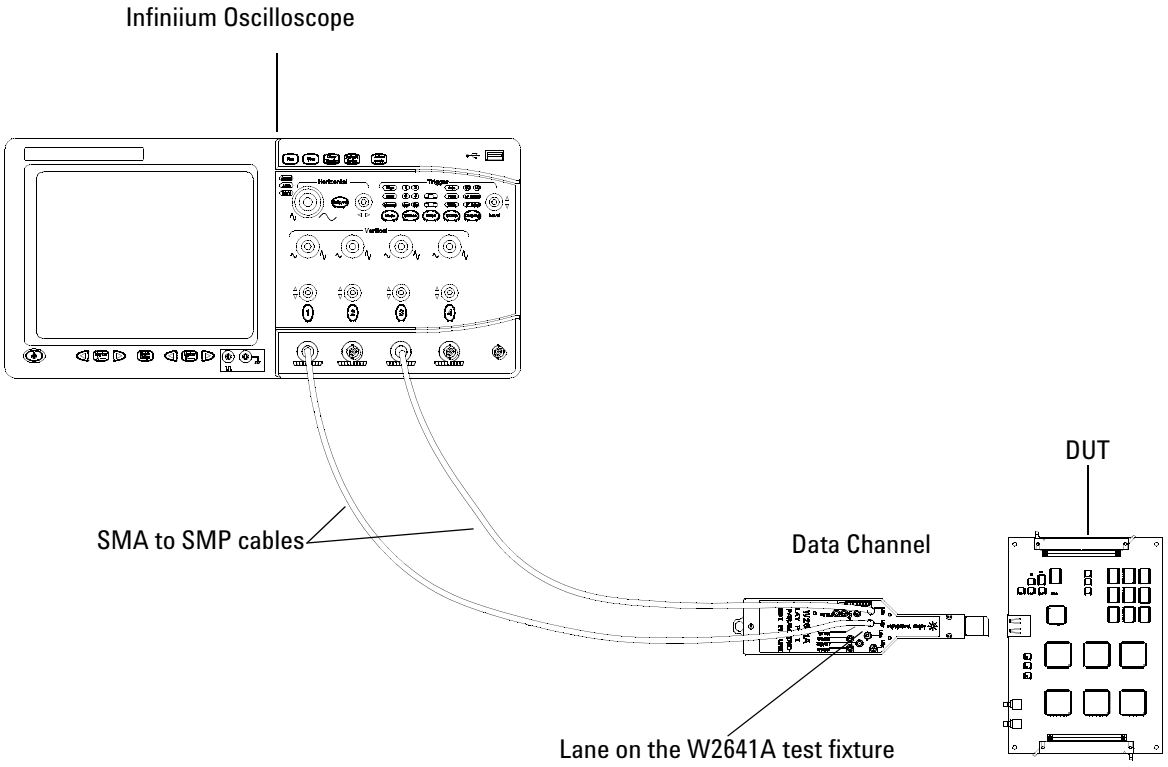

Figure 45 Differential Measurement Setup Using Two Single Ended Connections - SSC Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see Chapter 30, “InfiniiMax Probing,” starting on page 299.

Source Spread Spectrum Clocking (SSC) Differential Test

Spread Spectrum Modulation Frequency (Normative)

The spread spectrum modulation frequency evaluates the frequency of the SSC modulation and validates if it falls with specification limits.

The SSC frequency will be evaluated at the highest bit rate the transmitter supports. Tests shall be performed on a PRBS 7 signal, with SSC enabled. An evaluation of at least 10 full SSC cycles is required (Mean value reported). As SSC is mandatory, the reported result must be the mean of ten measured with maximum values from the range of SSC modulation deviation.

Spread Spectrum Modulation Deviation (Normative)

The spread spectrum modulation deviation evaluates the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [the device must] operate in the region of 0 to -5000 PPM. The SSC Modulation Deviation will be evaluated at the highest bit rate the transmitter supports. Tests shall be performed on a PRBS 7 signal, with SSC enabled.

An evaluation of at least 10 full SSC cycles is required (Mean value reported). As SSC is mandatory, the reported result must be the mean of ten measured with maximum values from the range of SSC modulation deviation.

The value reported as the result must be the single total range value relative to nominal of the SSC modulation deviation, using the equation below, where "Min" is the mean of 10 recorded values of the minimum peaks.

Calculate deviation = (Measured Min - Nominal)/Nominal * 1e6 ppm

Deviation HF Variation (Informative)

The deviation HF variation verifies SSC profile that does not include any frequency deviations which would exceed 1250 ppm/µSec.

Spread spectrum clocking demands that the sink receiver tracks the modulated frequency of the source link rate while maintaining clock/data phase tracking. This test measures the range of frequency deviation with the source SSC enabled. If this range exceeds specification, the ability of the sink to frequency and phase track may be impaired, possibly causing data recovery errors and non-interoperability with a compliant receiver.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. SSC tests are available in the 2 test modes only- User Defined Conditions and Targeted Characterization Testing.
8. The Deviation HF Variation test is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked for this test.

Navigate to the Spread Spectrum Clocking (SSC) group and select the appropriate test and the lane number to be tested.

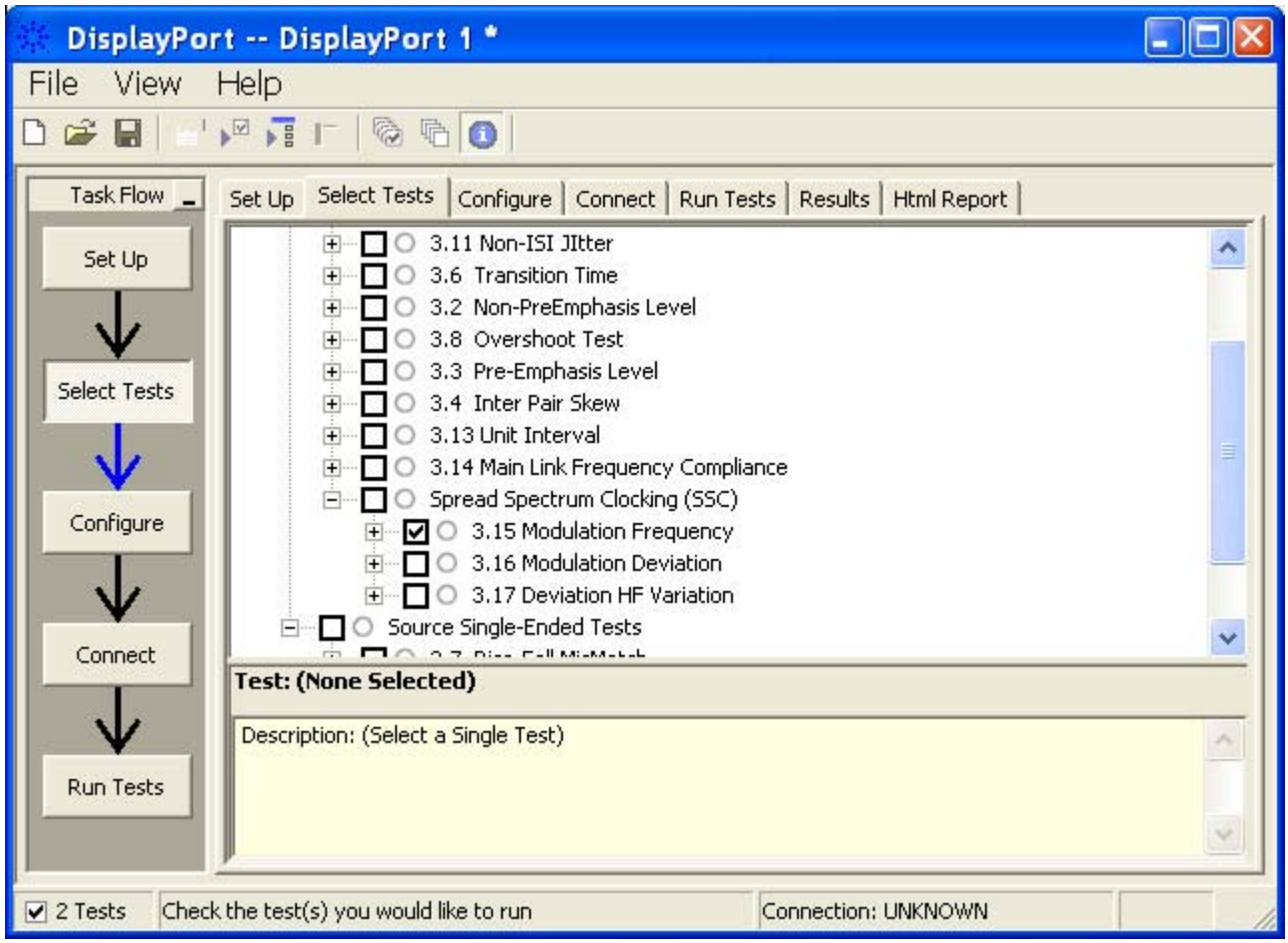

Figure 46 Selecting the Spread Spectrum Clocking (SSC) Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 20), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 20 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	

Table 20 Test Configuration Options

Configuration Option	Description
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

SSC Modulation Frequency Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Modulation Deviation Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Deviation HF Variation Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Modulation Frequency PASS Condition

The SSC Modulation Frequency result must satisfy the following criteria:

- f_{SSC} measures between 30 kHz and 33 kHz

  The value above shall be based on a mean of at least 10 complete SSC cycles.

SSC Modulation Deviation PASS Condition

The SSC Modulation Deviation result must satisfy the following criteria:

- SSC_{tol} measures between 5000 ppm and 0 ppm

  The value above shall be based on a mean of at least 10 complete SSC cycles.

SSC Deviation HF Variation PASS Condition

The SSC Deviation HF Variation result must satisfy the following criteria:

- SSCt dF/dt ≤ 1250 ppm/µSec variations

The value above shall be based on a mean of at least 10 complete SSC cycles.

Test References

See Test 3.15: Spread Spectrum Modulation Frequency, Test 3.16: Spread Spectrum Modulation Deviation and Test 3.17: Deviation HF Variation in the *DisplayPort- Compliance Test Specification Version 1.1.*

15 Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)

16 Source Rise-Fall Mismatch Single-Ended Tests (Informative)

This section provides the guidelines for source rise-fall mismatch single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Rise-Fall Mismatch Single-Ended Tests

When performing the rise-fall mismatch test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 47 below shows the single-ended connections for the Rise-Fall Mismatch Single-Ended Tests.

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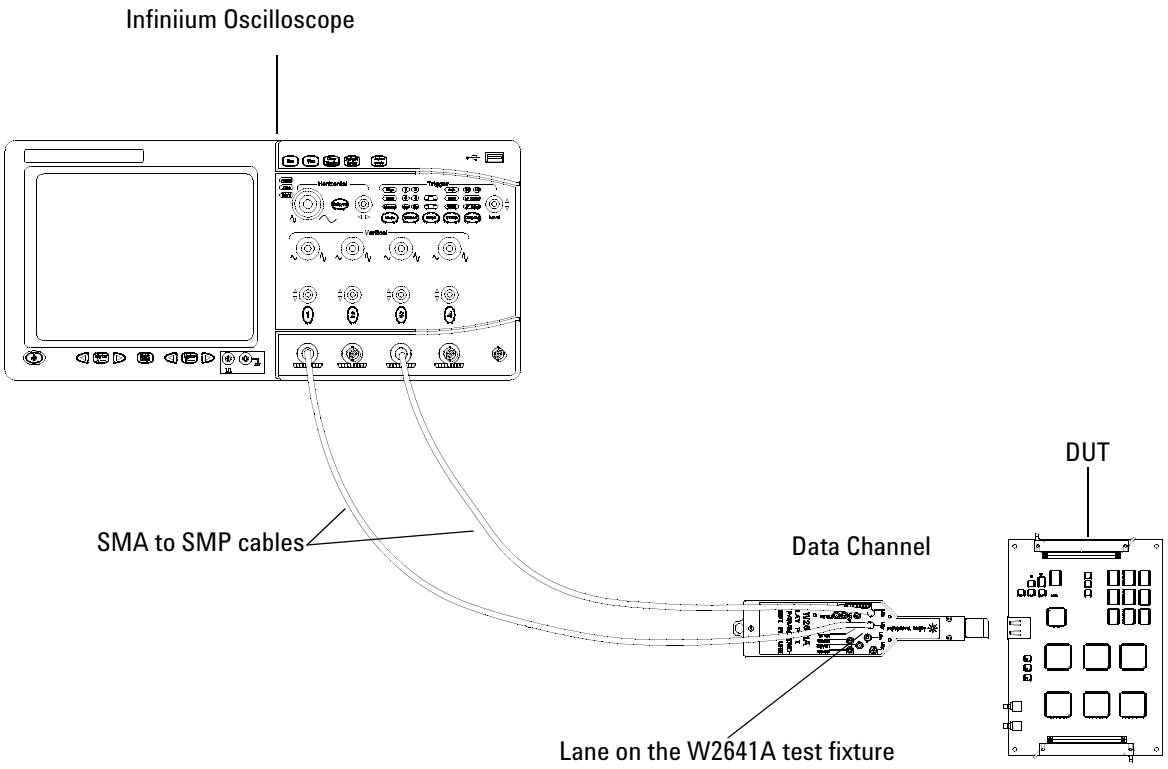

Figure 47 Differential Measurement Setup Using Two Single Ended Connections - Rise-Fall Mismatch Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source Rise-Fall Mismatch Single-Ended Tests

The rise and fall time mismatch tests evaluate the differences in rise and fall times of the two single-ended waveform in a given differential data lane of a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard specification).

The mismatch in time of the rising and falling time of the single-ended signals composing a differential lane will create common mode noise and will radiate.

The rise and fall times are measured between the 80% and 20% levels of the waveform.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.
8. This is an Informative test, therefore, the Show Normative Tests Only checkbox must be un-checked.

Navigate to the Rise-Fall Mismatch group, and check the Rising Mismatch or Falling Mismatch tests that you want to perform and the lane number to be tested.

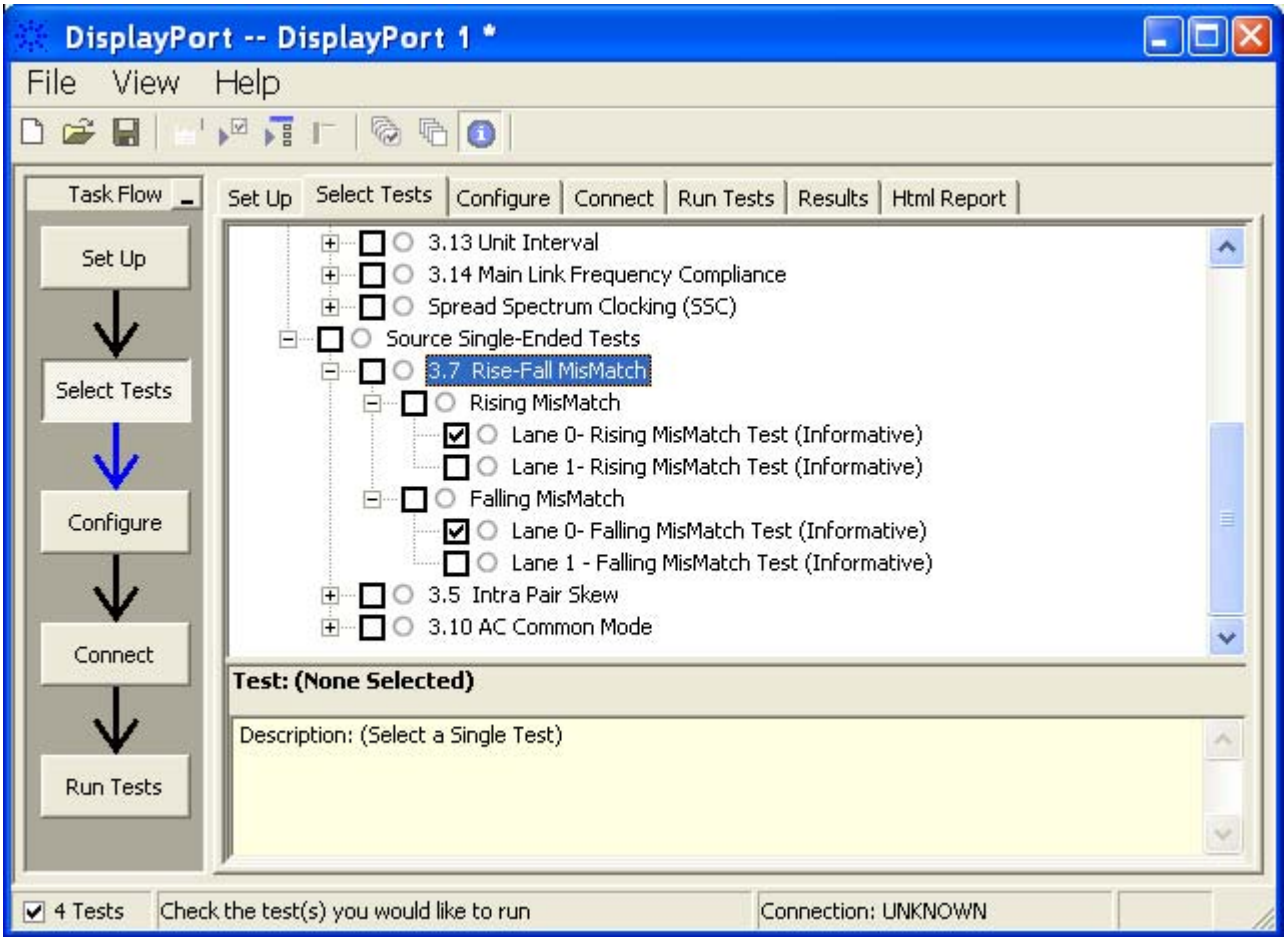

Figure 48 Selecting Rise-Fall Mismatch Tests

9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 21), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 21 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Single-ended Tests	
Rise-Fall Mismatch	

Table 21 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Threshold	Sets the threshold used to make a rise time or fall time measurement.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then SSC Disabled will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

Two single-ended signals are probed independently, acquired simultaneously and compared.

PASS Condition

Falling Mismatch ≤ 15% of the single-ended rise time
Rising Mismatch ≥ 15% of the single-ended fall time

Test References

See section 3.7, in the *DisplayPort- Compliance Test Specification Version 1.1*.

17
Source Intra Pair Skew Single-Ended Tests

This section provides the guidelines for source intra pair skew single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source Intra Pair Skew Single-Ended Tests

When performing the intra pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 49 below shows the single-ended connections for Intra Pair Skew Single-Ended Tests.

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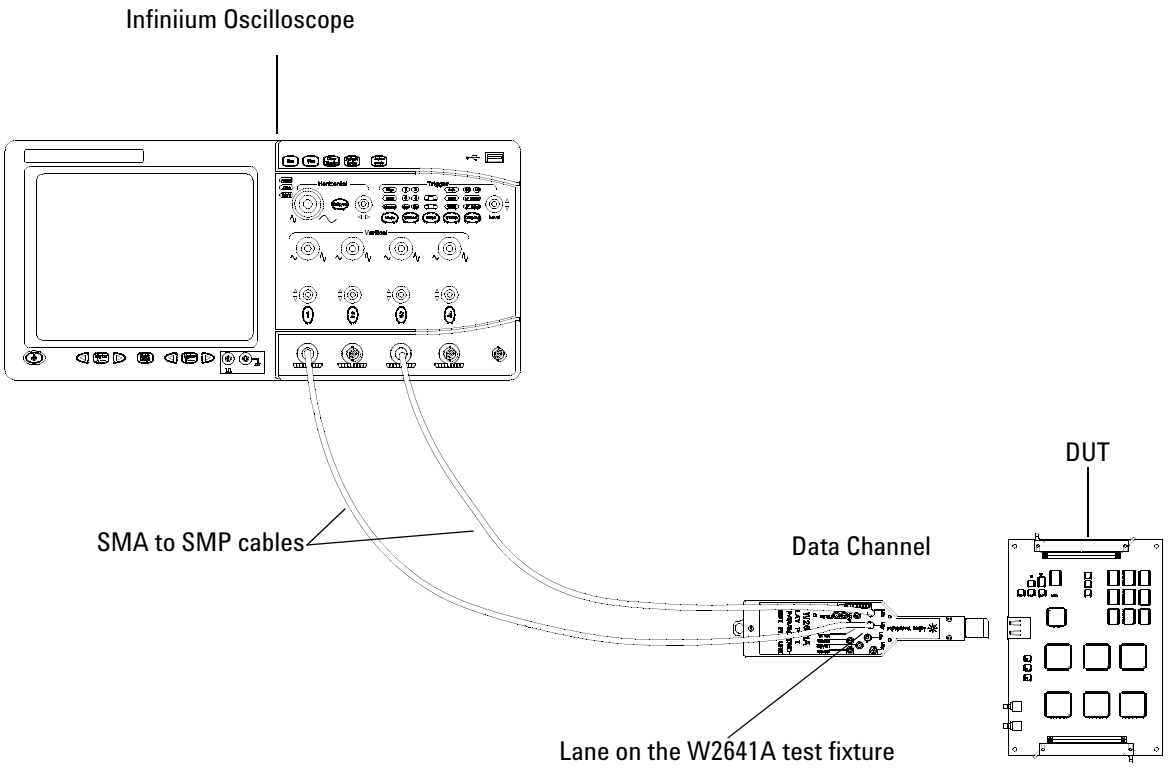

Figure 49 Differential Measurement Setup Using Two Single Ended Connections - Intra Pair Skew Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source Intra Pair Skew Single-Ended Tests

The intra pair skew test evaluates the skew, or time delay, between the respective sides of a differential data lane in a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard).

Intra pair skew has deleterious effects on signal rise time and manner of crossing through the transition point. The DisplayPort specification at package pins (TP1) is 20 ps. It can clearly double or triple to and through the connector. These are secondary contributors to source jitter performance.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Intra Pair Skew - Lane # - Intra Pair Skew Test where # is the lane number to be tested.

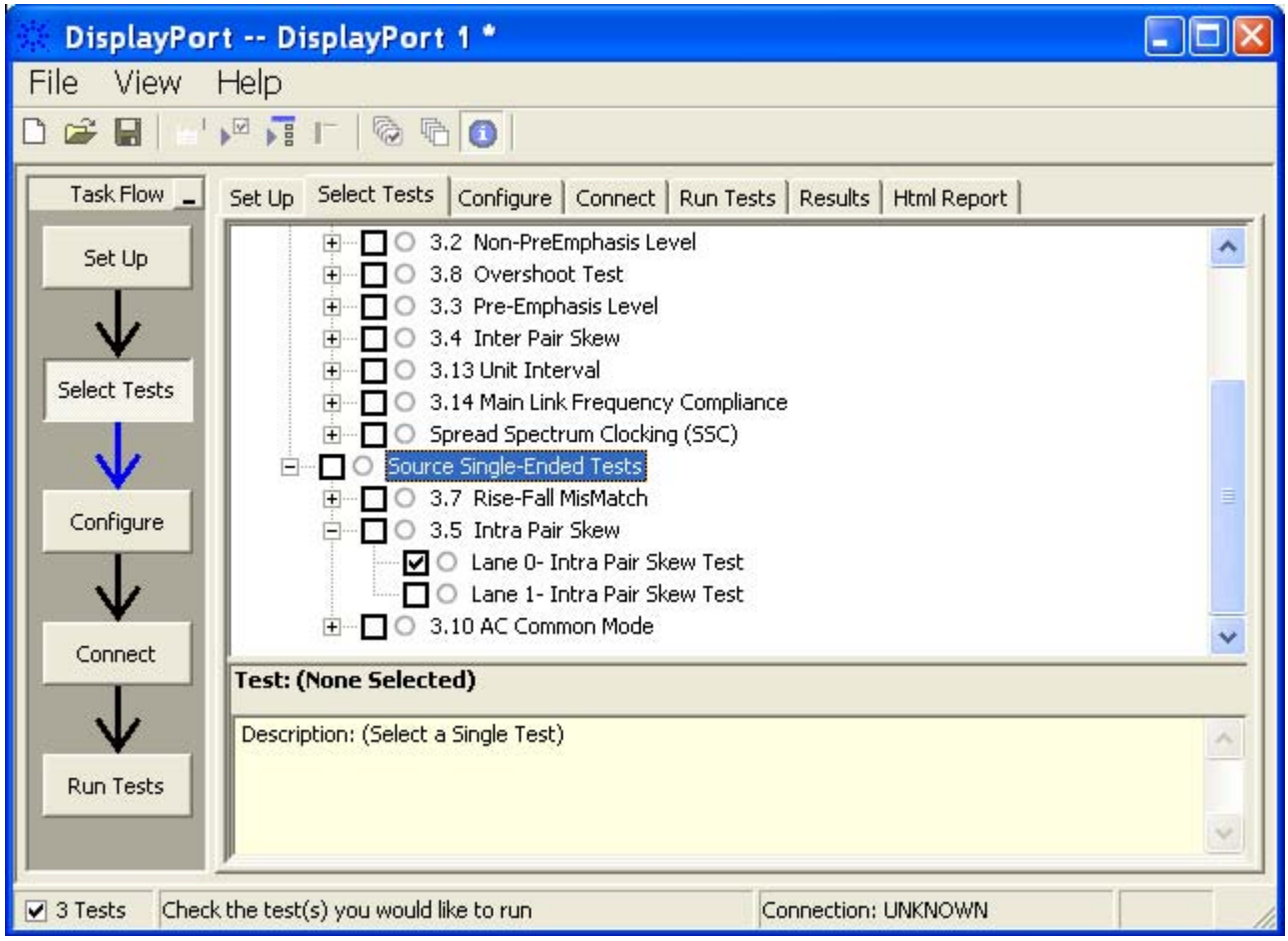

Figure 50 Selecting Intra Pair Skew Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 22), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 22 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Single-ended Tests	
Intra-pair Skew	
Intra Pair Skew Edges	Sets the number of edges measured for the intra pair skew test.

Table 22 Test Configuration Options

Configuration Option	Description
Skew Trigger Patterns	Define trigger pattern for intra pair skew test.

Test Condition

Bit Rate: highest bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then both will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Intra pair skew ≤ 30 ps

Test References

See Test 3.5: in the *DisplayPort- Compliance Test Specification Version 1.1.*

18 Source AC Common Mode Noise Single-Ended Tests

This section provides the guidelines for source AC common mode noise single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Source AC Common Mode Noise Single-Ended Tests

When performing the AC common mode noise test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 51 below shows the single-ended connections for AC Common Mode Noise Single-Ended Tests.

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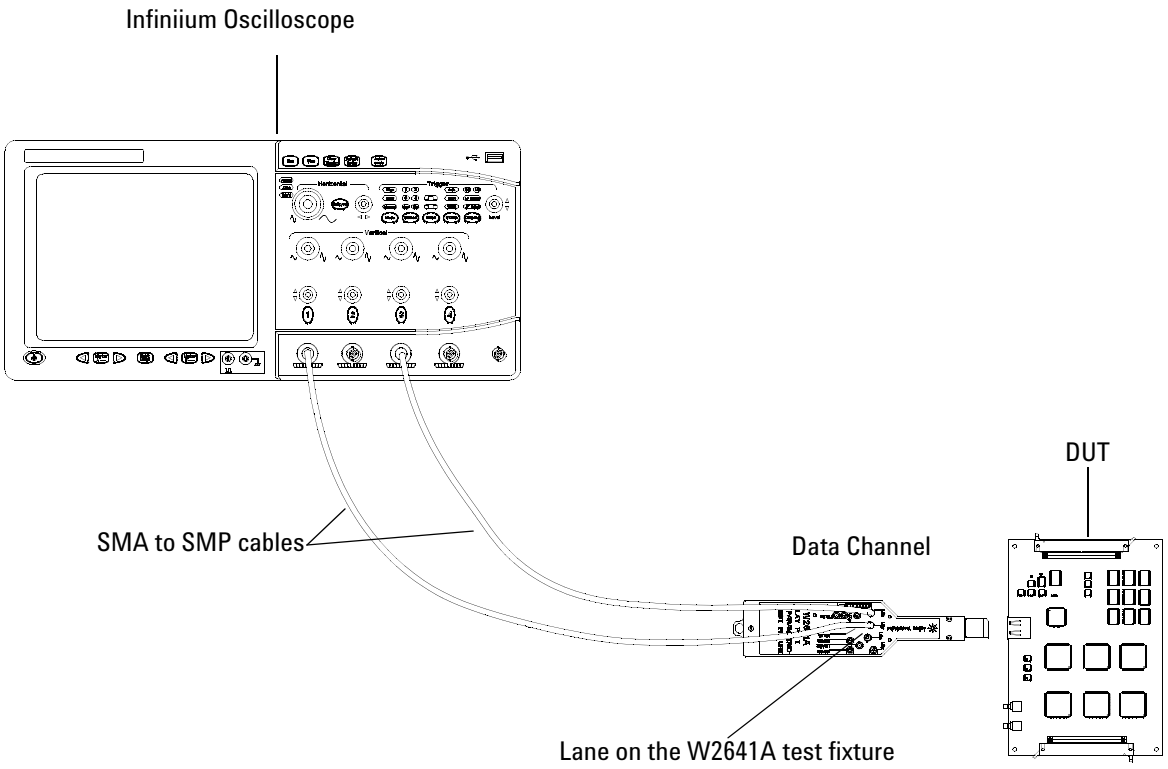

Figure 51 Differential Measurement Setup Using Two Single Ended Connections - AC Common Mode Noise Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source AC Common Mode Noise Single-Ended Test

The AC common mode noise measurement of the distributed clock network verifies that the nominal operating clock frequency is within the acceptable tolerance range. In order for the sink devices to properly recover the data, the source clock must operate within the acceptable tolerance range.

The test must be made at all bit rates supported by the device under test without pre-Emphasis and a voltage swing of 1.2 volts. A test pattern of D10.2 should be used.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the AC Common Mode - Lane # - Common Mode AC Test where # is the lane number to be tested.

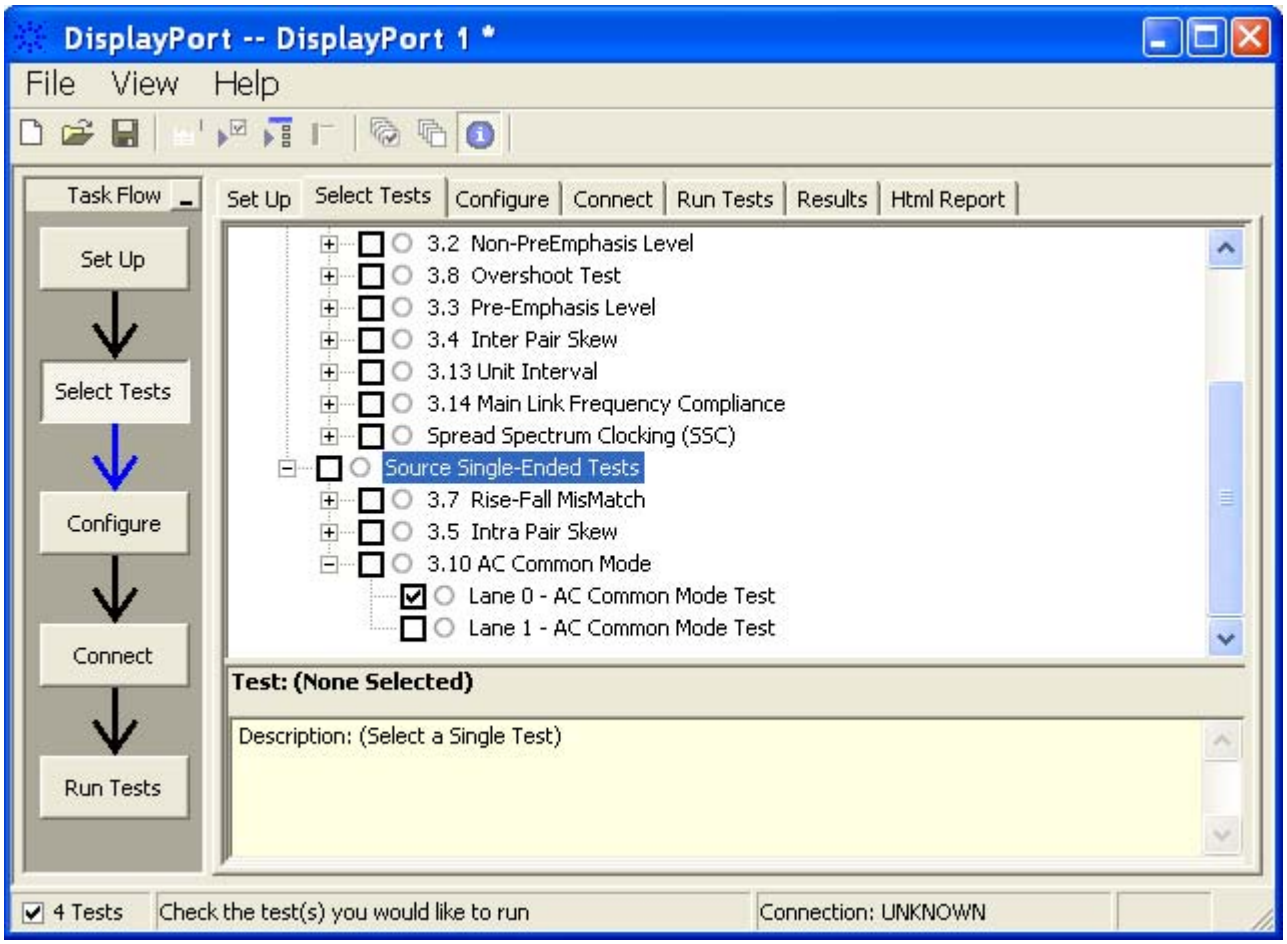

Figure 52 Selecting AC Common Mode Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 23), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 23 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Single-ended Tests	
AC Common Mode	

Table 23 Test Configuration Options

Configuration Option	Description
AC Common Edge	Sets the number of edges measured for the AC common mode test.
Interpolation	Specifies whether to turn on or off the Sin(x)/x interpolation. Turning On interpolation may cause more peak-to-peak jitter.
Filter	Specifies whether a high pass filter, low pass filter or no filter is applied before the measurement. Interpolation is turned off if any filter is chosen.
Cut Off Frequency	Sets the Cut Off Frequency if a Filter is applied.Specify in correct format; xMHz, xkHz or xHz.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: all the pre-Emphasis settings are supported.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then SSC Disabled will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

Two single-ended signals are probed independently, acquired simultaneously and compared.

PASS Condition

AC Common Mode Noise ≤ 20 mVrms.

Test References

See Test 3.10: AC Common Mode Noise, in the *DisplayPort- Compliance Test Specification Version 1.1*.

19 Link Layer Phy Change Tests

This section provides the guidelines for link layer phy change tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application. Link layer phy change tests are not compliance tests. The purpose of these tests is to verify if the link layer phy change is operating properly prior to any tests. These tests verify if the DUT is able to respond well when the configuration of the link layer is changed.

Probing for Link Layer Phy Change Tests

When performing the link layer phy change test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 53 below shows the single-ended connections for Link Layer Phy Change Tests.

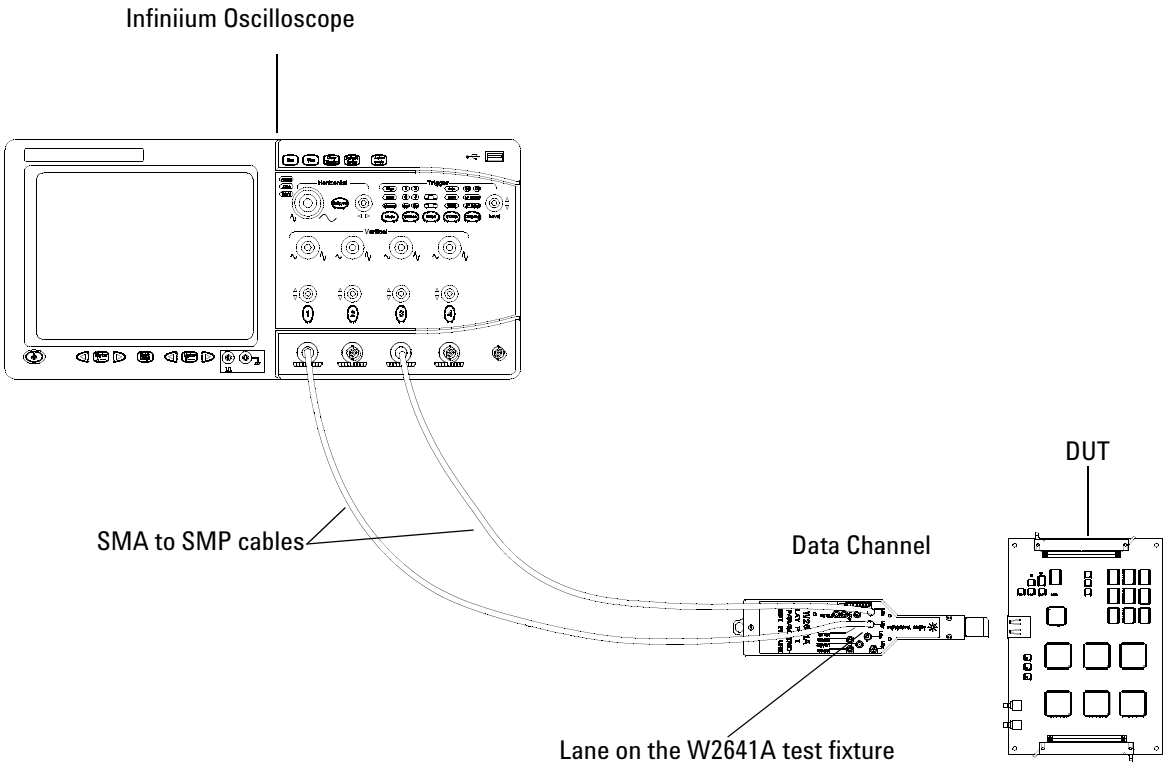

Figure 53 Differential Measurement Setup Using Two Single Ended Connections - Link Layer Phy Change Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Link Layer Phy Change Tests

The link layer phy change tests consists of Pre-Emphasis, Level and Bit Rate tests.

Link Layer Phy Change - Pre-Emphasis

The link layer - pre-Emphasis test verifies if the pre-Emphasis of the DUT can change accordingly from the lowest pre-Emphasis to the highest pre-Emphasis setting.

The test must be made on the highest bit rate supported by the differential voltage swings of 400 mV using a test pattern of PRBS 7. The following equation is used to calculate the pre-Emphasis result:

Pre-Emphasis Result = 20log(VSwingPE/ VSwingNoPE)

VSwingPE = VHpe-VLpe

VSingNoPE = VHnope-VLnope

where:

VHpe = the high voltage value is measured using the histogram modes at the top for transition eyes.

VLpe = the low voltage value is measured using the histogram modes at the top for transition eyes.

VHnope = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

VLnope = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

Link Layer Phy Change - Level

The link layer - level tests verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.

The amplitude measurement is performed using the following equation at all bit rates without pre-Emphasis and a PRBS 7 waveform:

Peak-to-peak Voltage = VH - VL where:

VH is the high voltage levelVL is the low voltage level

Link Layer Phy Change - Bit Rate

The link layer - bit rate tests verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.

The test must be made at all bit rates supported by the DUT without pre-Emphasis and a voltage swing of 400 mV. A test pattern of PRBS 7 should be used.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Link Layer (Phy Change Test) group, and check the test and lane you want to test.

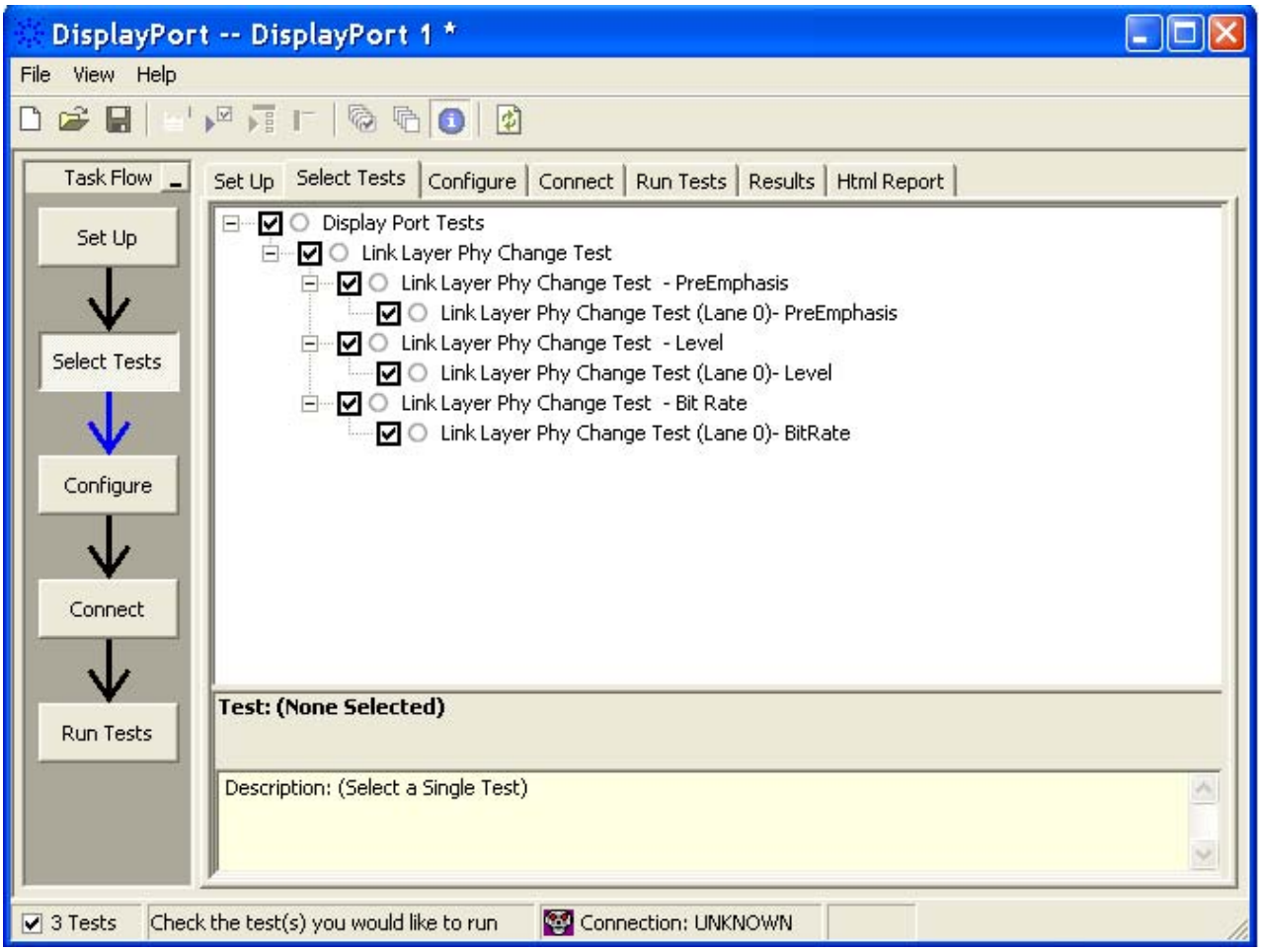

Figure 54 Selecting Link Layer Phy Change Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 24), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 24 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Pre-Emphasis Test Condition

Bit Rate: highest bit rates are supported.

Output Level: 400 mVolts.

Pre-Emphasis: All.

Test Pattern: PRBS 7.

Level Test Condition

Bit Rate: highest bit rates are supported.

Output Level: All.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

Bit Rate Test Condition

Bit Rate: all bit rates are supported.

Output Level: 400 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

Pre-Emphasis PASS Condition

Link Layer Phy Change - Pre-Emphasis Test

For 3.5 dB setting: Resultant3.5dB $\geq$ 2.0 dB

For 6.0 dB setting: Resultant6.0dB results $\geq$ Resultant3.5dB + 1.6

For 9.5 dB setting: Resultant9.5dB results $\geq$ Resultant6.0dB + 1.6

Level PASS Condition

Link Layer Phy Change - Level Test

Output Level 1: 340 mV $\leq$ Voltage Peak-Peak $\leq$ 460 mV

Output Level 2: 510 mV $\leq$ Voltage Peak-Peak $\leq$ 680 mV

Output Level 3: 690 mV $\leq$ Voltage Peak-Peak $\leq$ 920 mV

Output Level 4: 1020 mV $\leq$ Voltage Peak-Peak $\leq$ 1380 mV

Bit Rate PASS Condition

Link Layer Phy Change - Bit Rate Test

0.9 * Nominal Bit Rate < Measured Data Rate < 1.1 * Nominal Bit Rate

Test References

-

20
Sink Eye Diagram Tests

This section provides the guidelines for sink eye diagram tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Sink Eye Diagram Tests

When performing the sink eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 55 and Figure 56 show a physical connection for making differential and single-ended connections.

.

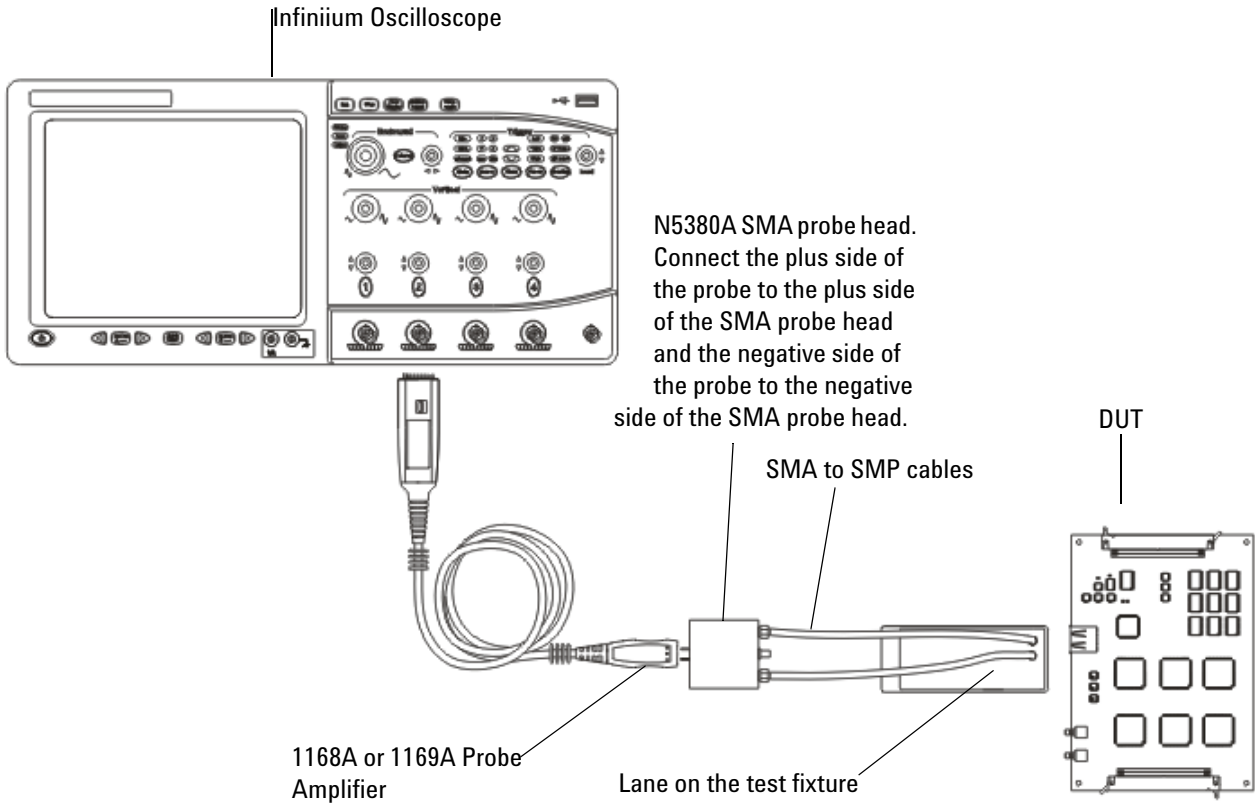

Figure 55 Probing for Differential Tests - Sink Eye Diagram Tests (Single Connection with DisplayPort Test Fixture)

.

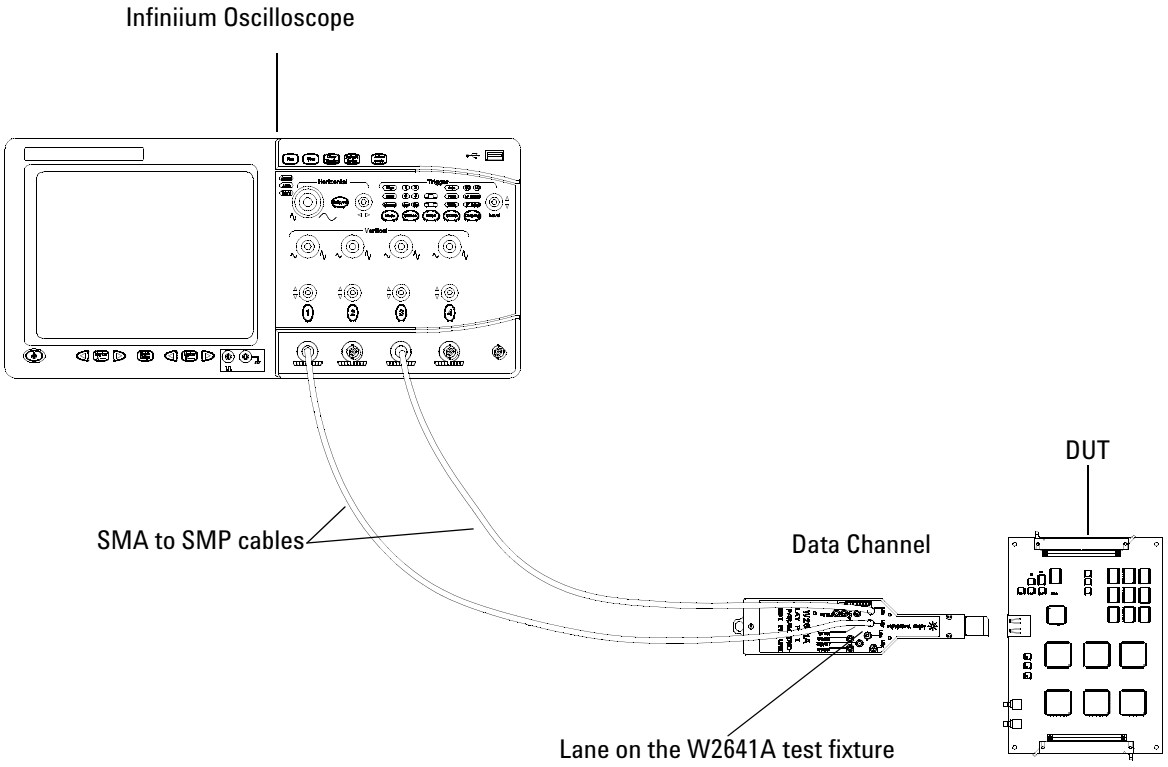

Figure 56 Differential Measurement Setup Using Two Single Ended Connections - Sink Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see Chapter 30, “InfiniiMax Probing,” starting on page 299.

Sink Eye Diagram Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in the transmitted data. The test must use a PRBS 7 test pattern at all voltage levels. The test should be performed without pre-Emphasis.

The sink eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Eye Diagram Test - Lane # - Sink Eye Diagram Test where # is the lane number to be tested.

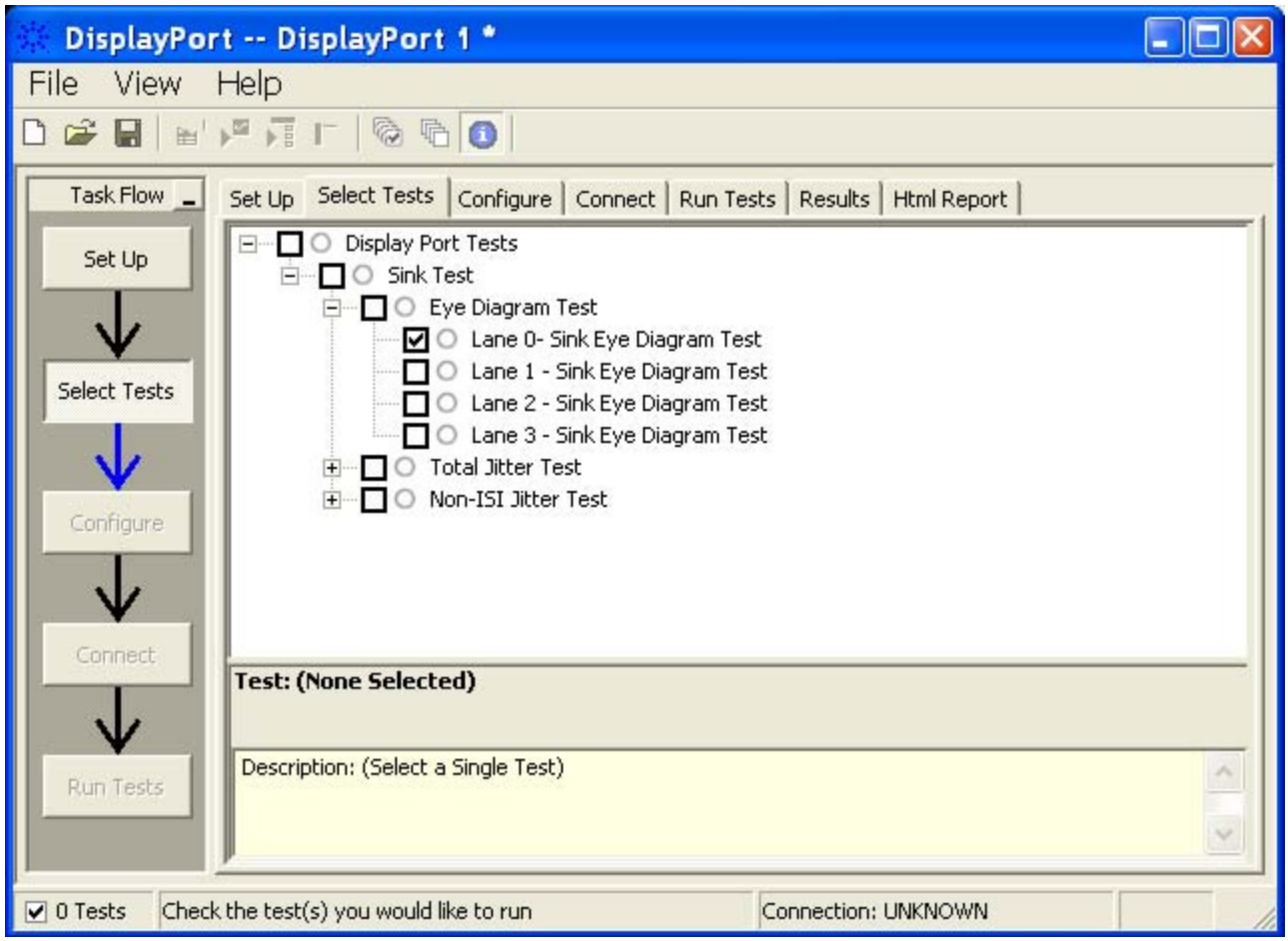

Figure 57 Selecting Sink Eye Diagram Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 25), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 25 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Sink Test	
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.

Table 25 Test Configuration Options

Configuration Option	Description
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

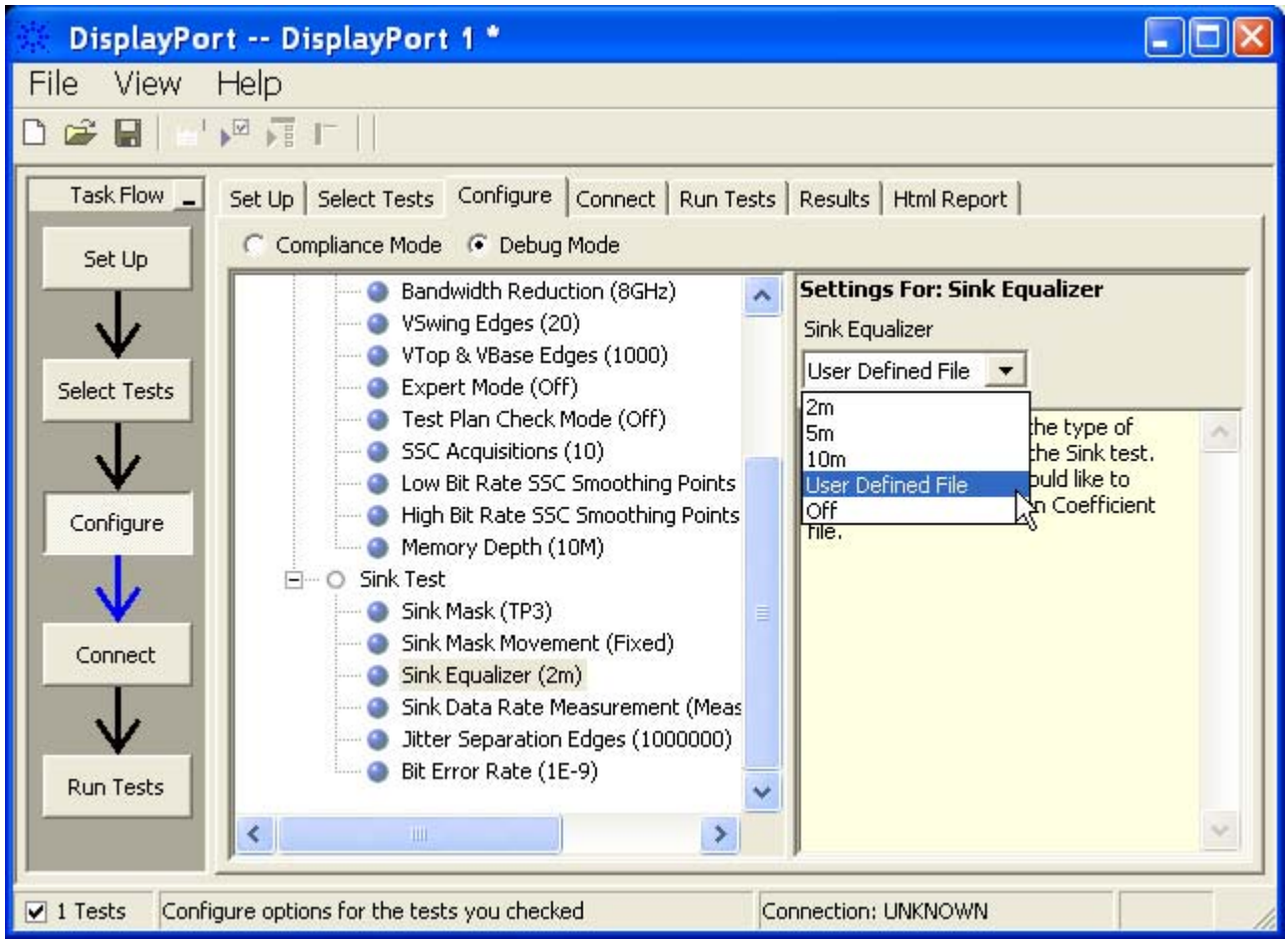

Figure 58 Selecting User Defined File for the Sink Equalizer

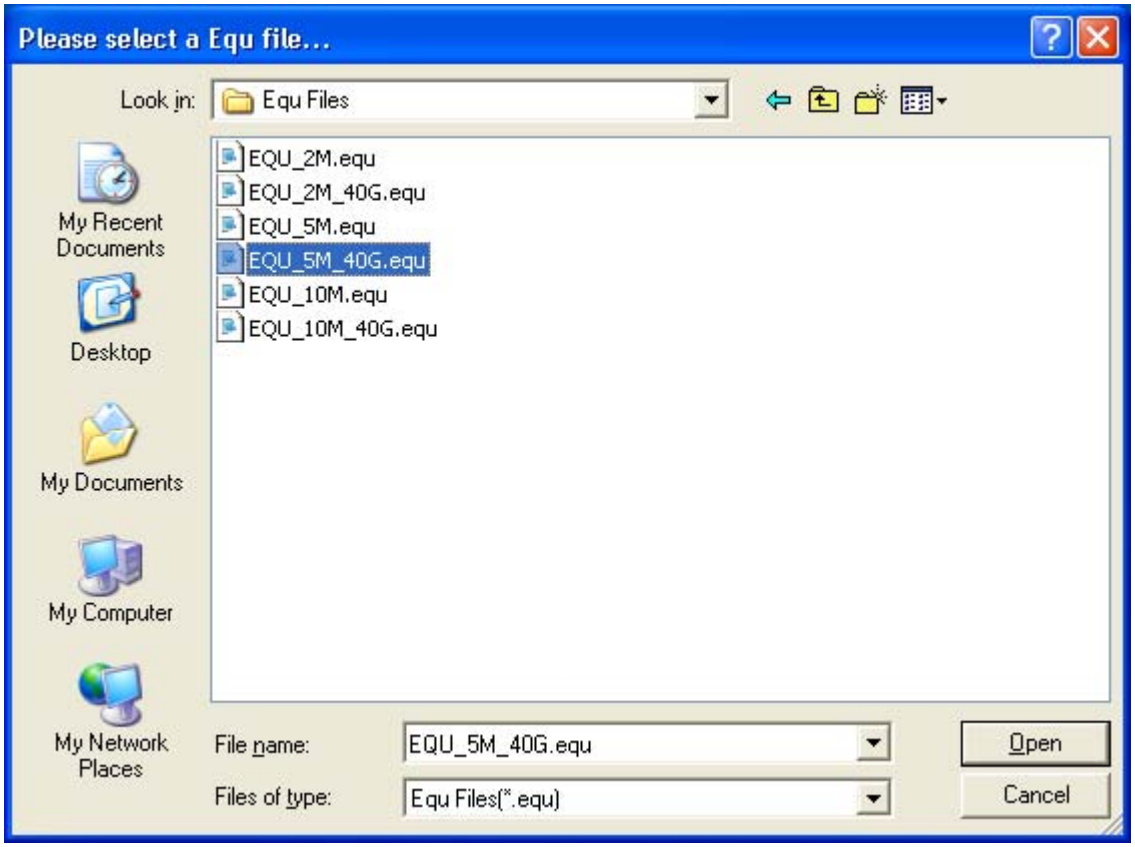

Figure 59 Selecting User Defined File

10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 26 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 26 Sink Eye Vertices for TP3

	Bit Rate	
Mask Point	**Reduced (1.6 Gb/s)**	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

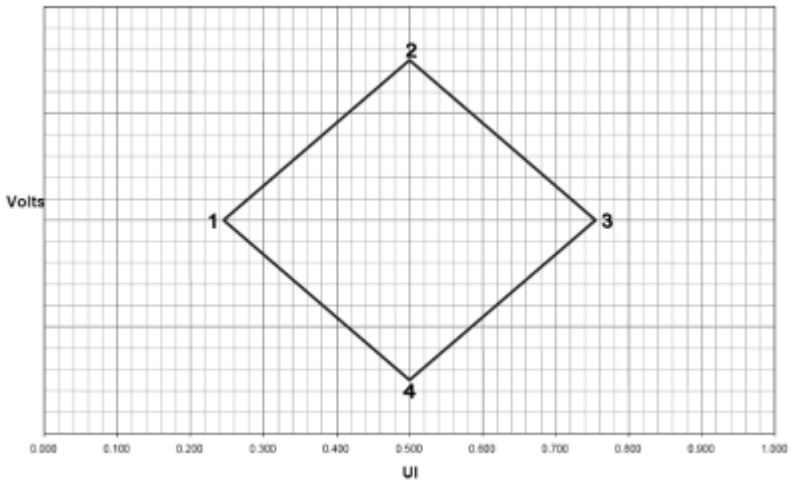

Figure 60 The Sink Eye Mask at TP3

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.1.*

21
Sink Total Jitter Tests

This section provides the guidelines for sink total jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Sink Total Jitter Tests

When performing the sink total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 61 and Figure 62 show a physical connection for making differential and single-ended connections.

.

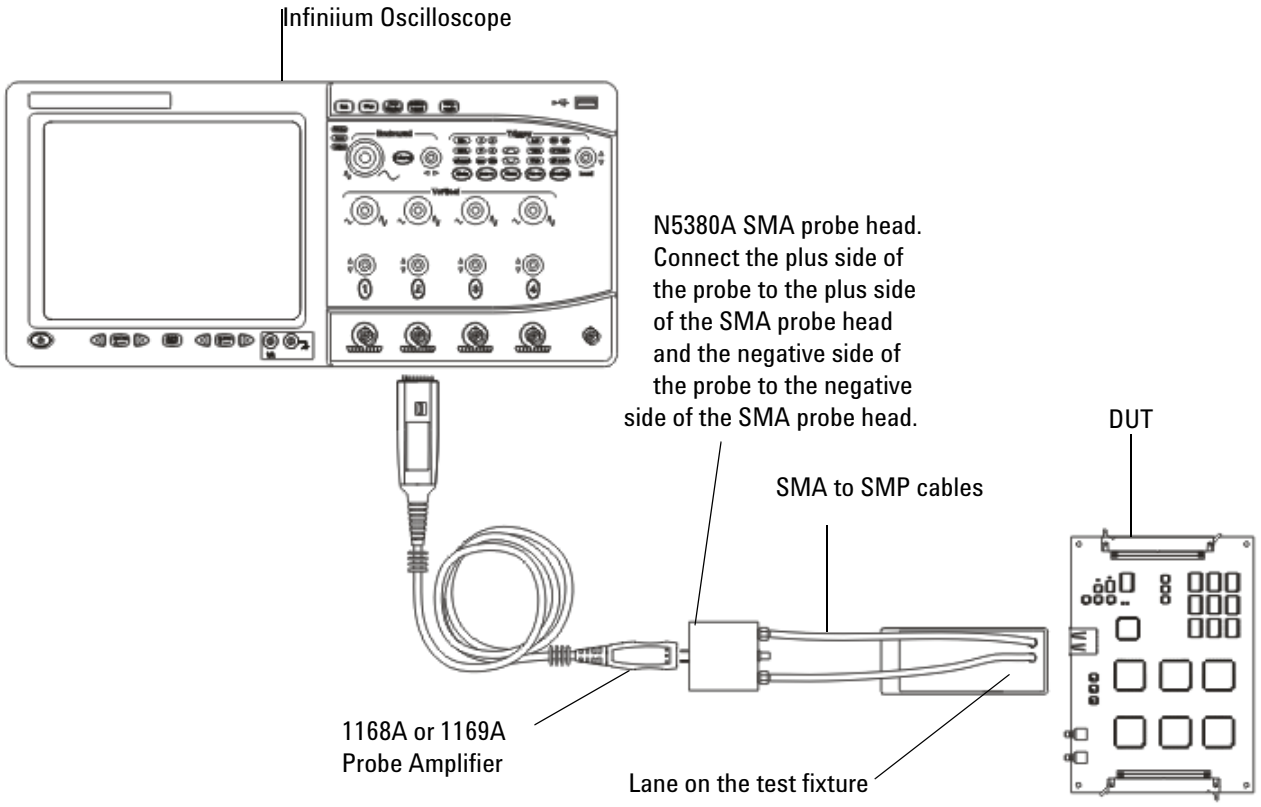

Figure 61 Probing for Differential Tests - Sink Total Jitter Tests (Single Connection with DisplayPort Test Fixture)

.

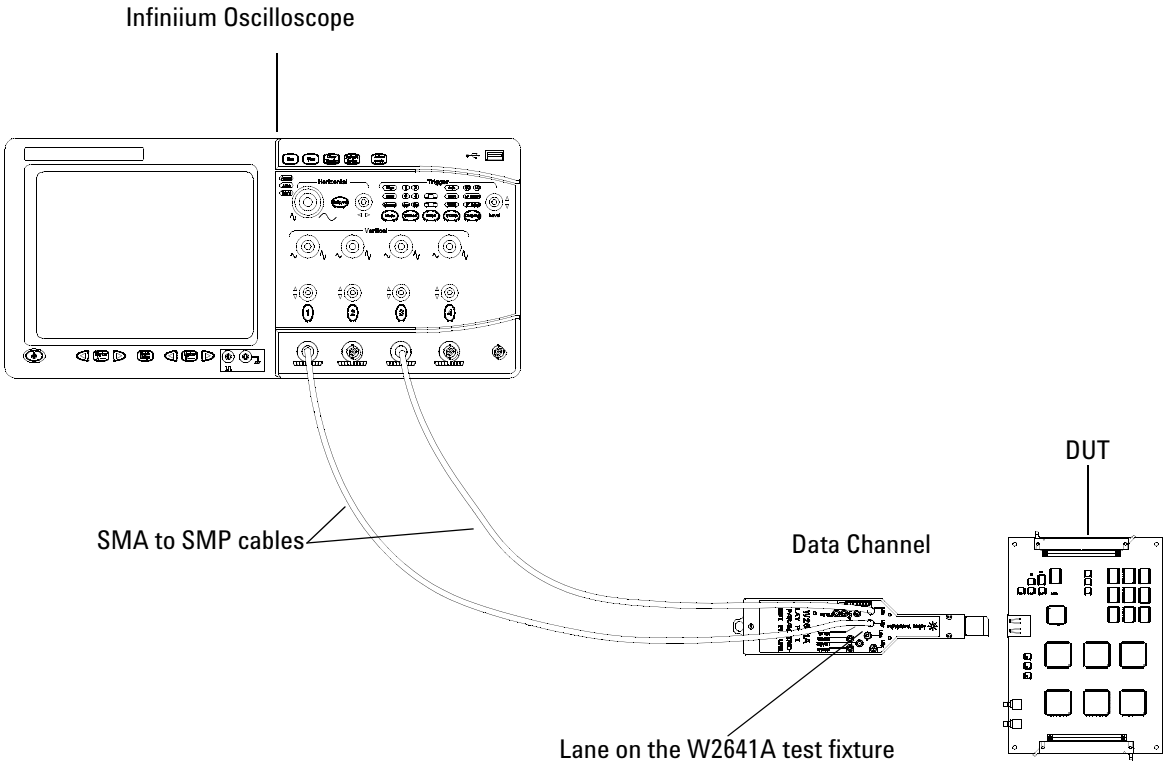

Figure 62 Differential Measurement Setup Using Two Single Ended Connections - Sink Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Sink Total Jitter Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Total Jitter Test - Lane # - Sink Total Jitter Test where # is the lane number to be tested.

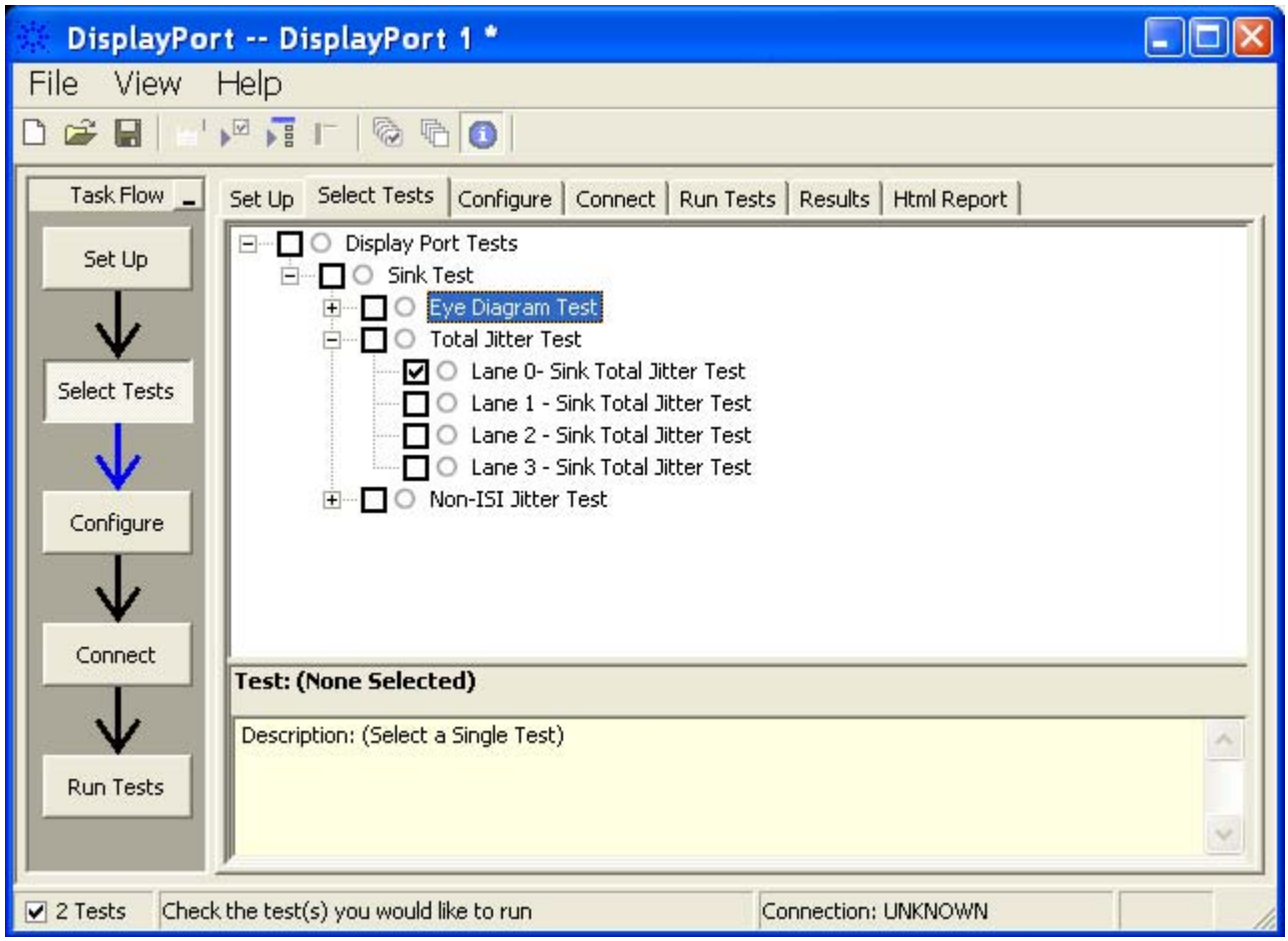

Figure 63 Selecting Sink Total Jitter Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 27), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 27 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Sink Test	
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.

Table 27 Test Configuration Options

Configuration Option	Description
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

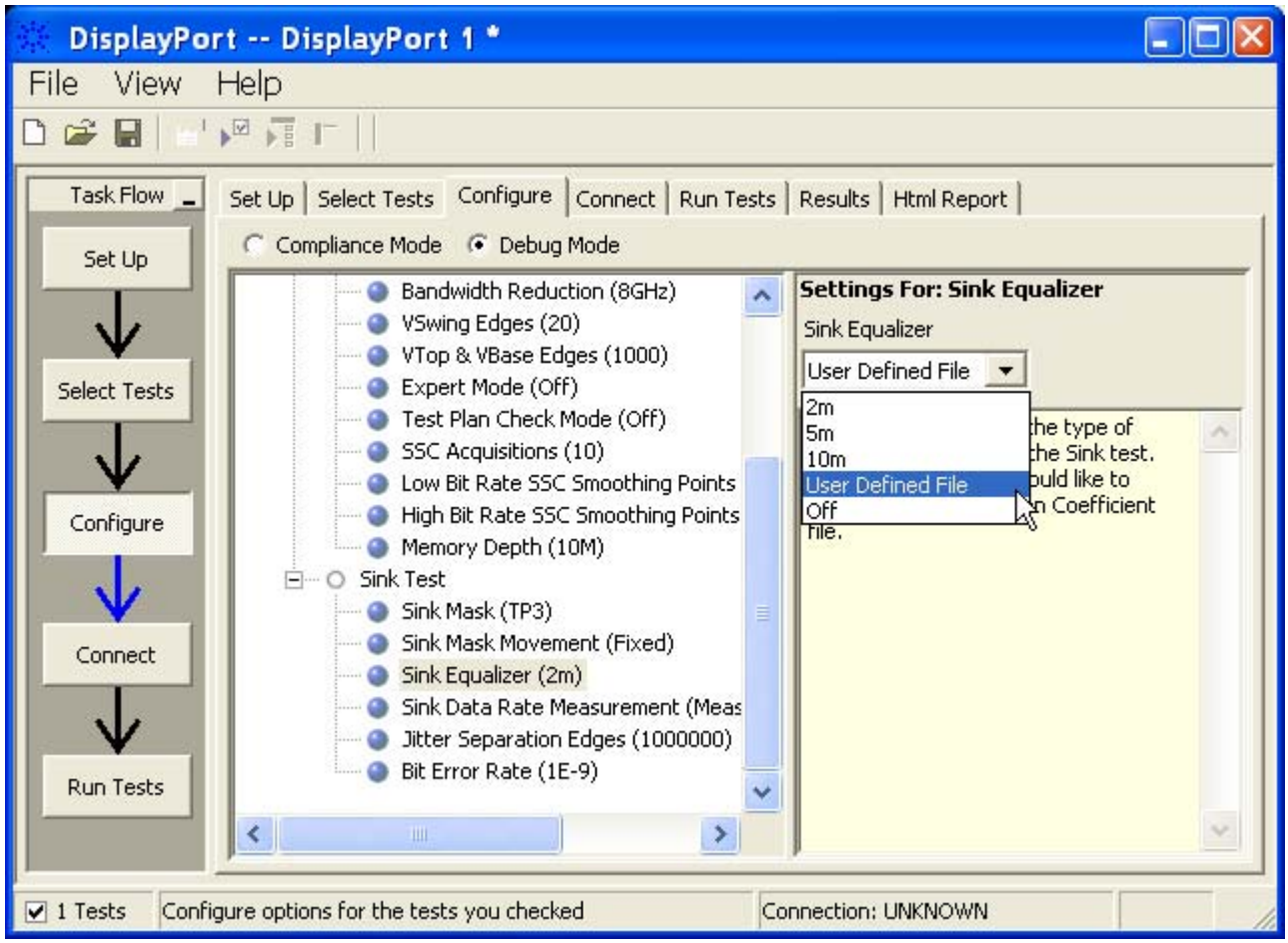

Figure 64 Selecting User Defined File for the Sink Equalizer

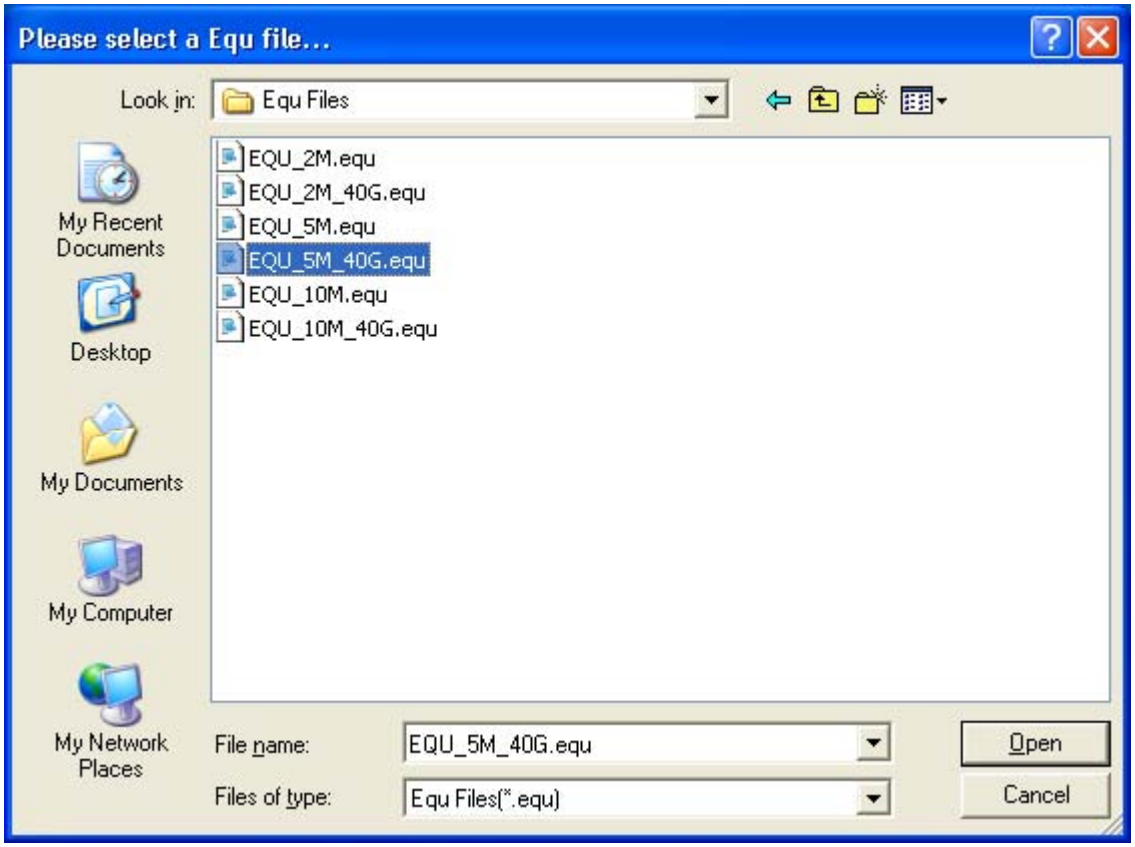

Figure 65 Selecting User Defined File

10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

-

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.1.*

22
Sink Non-ISI Jitter Tests

This section provides the guidelines for sink non-ISI jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Sink Non-ISI Jitter Tests

When performing the sink non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 66 and Figure 67 show a physical connection for making differential and single-ended connections.

.

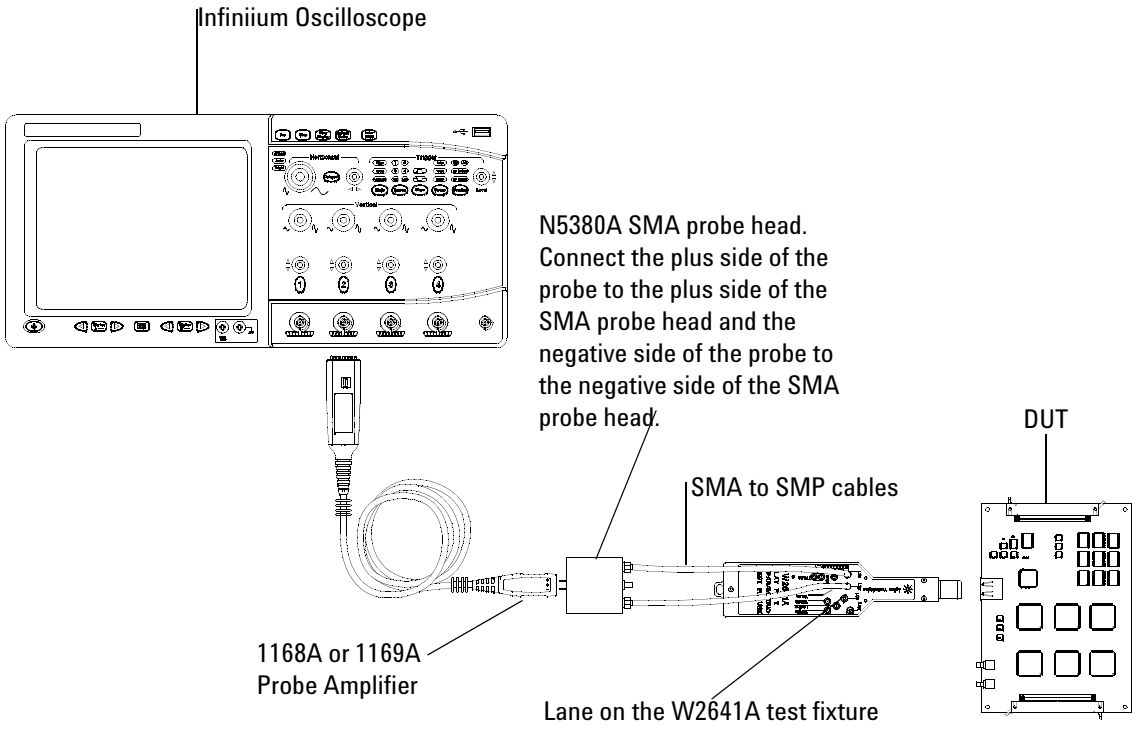

Figure 66 Probing for Differential Tests - Sink Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

.

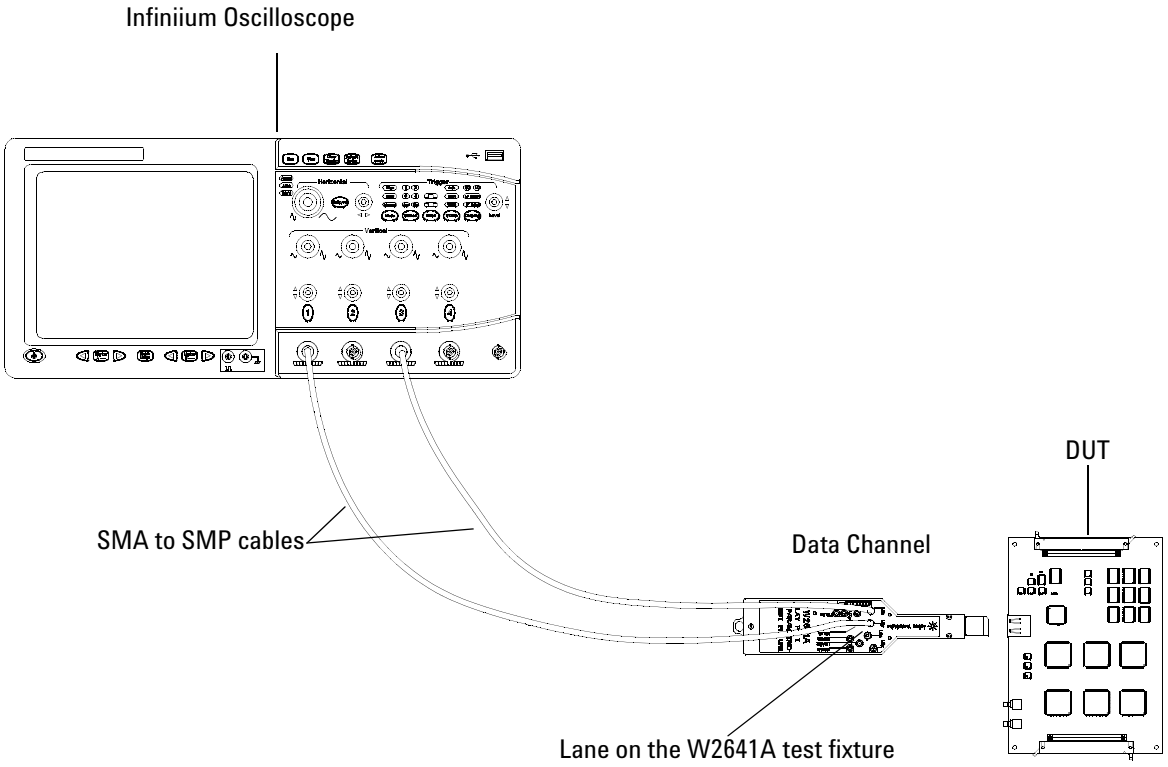

Figure 67 Differential Measurement Setup Using Two Single Ended Connections - Sink Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Sink Non-ISI Jitter Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Non-ISI Jitter Test - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

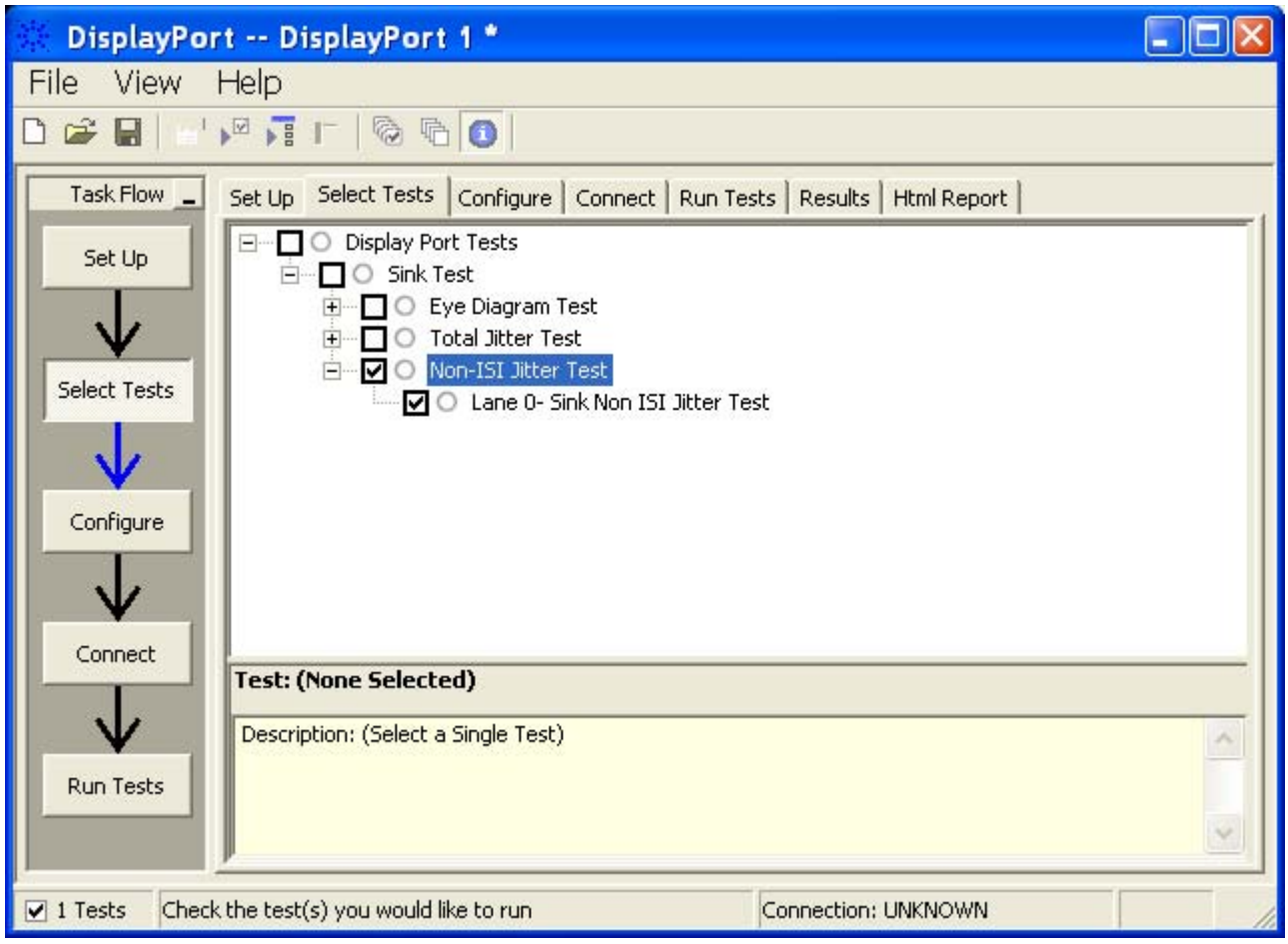

Figure 68 Selecting Sink Non-Jitter Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 28), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 28 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
	Sink Test
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.

Table 28 Test Configuration Options

Configuration Option	Description
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

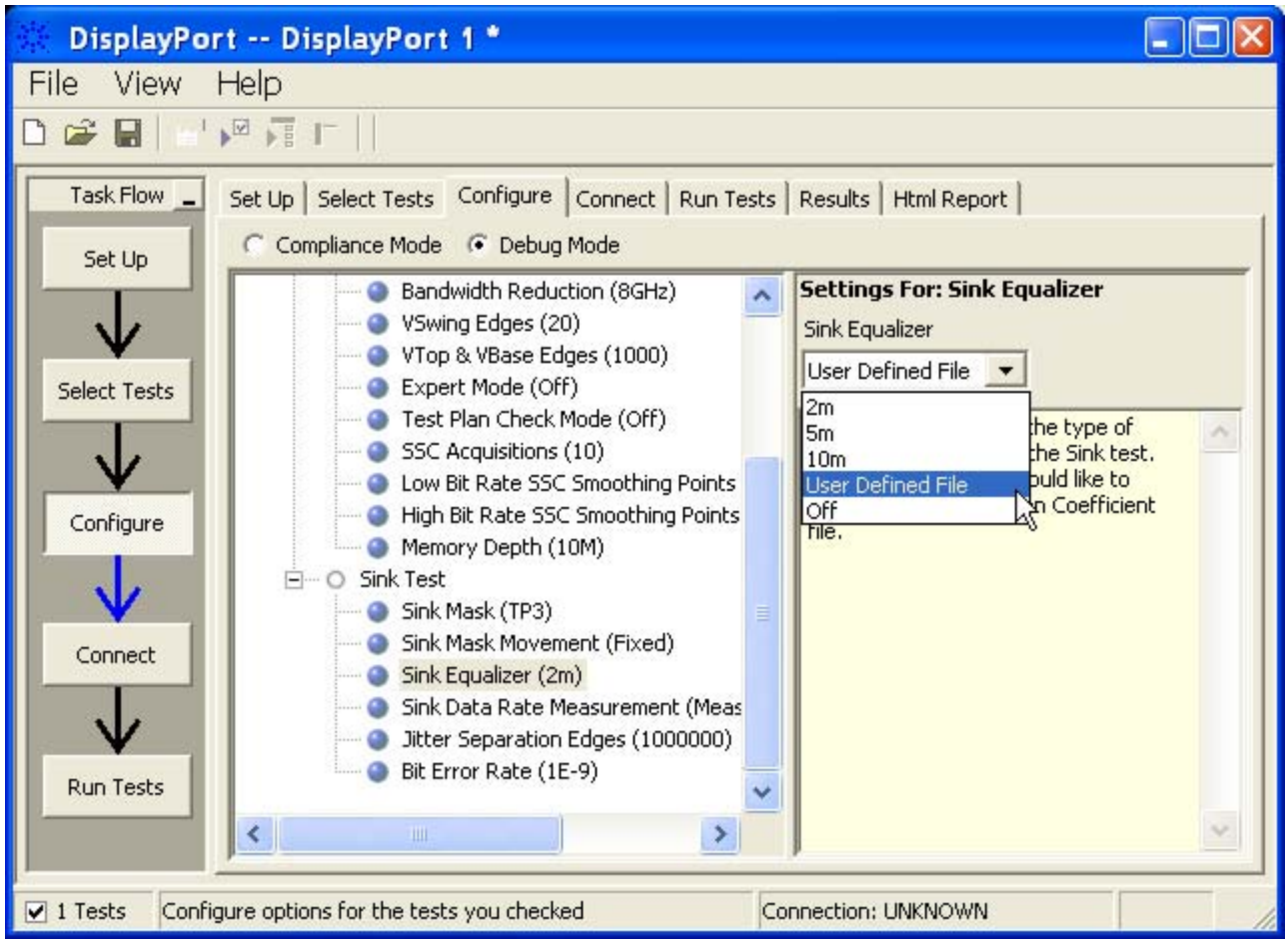

Figure 69 Selecting User Defined File for the Sink Equalizer

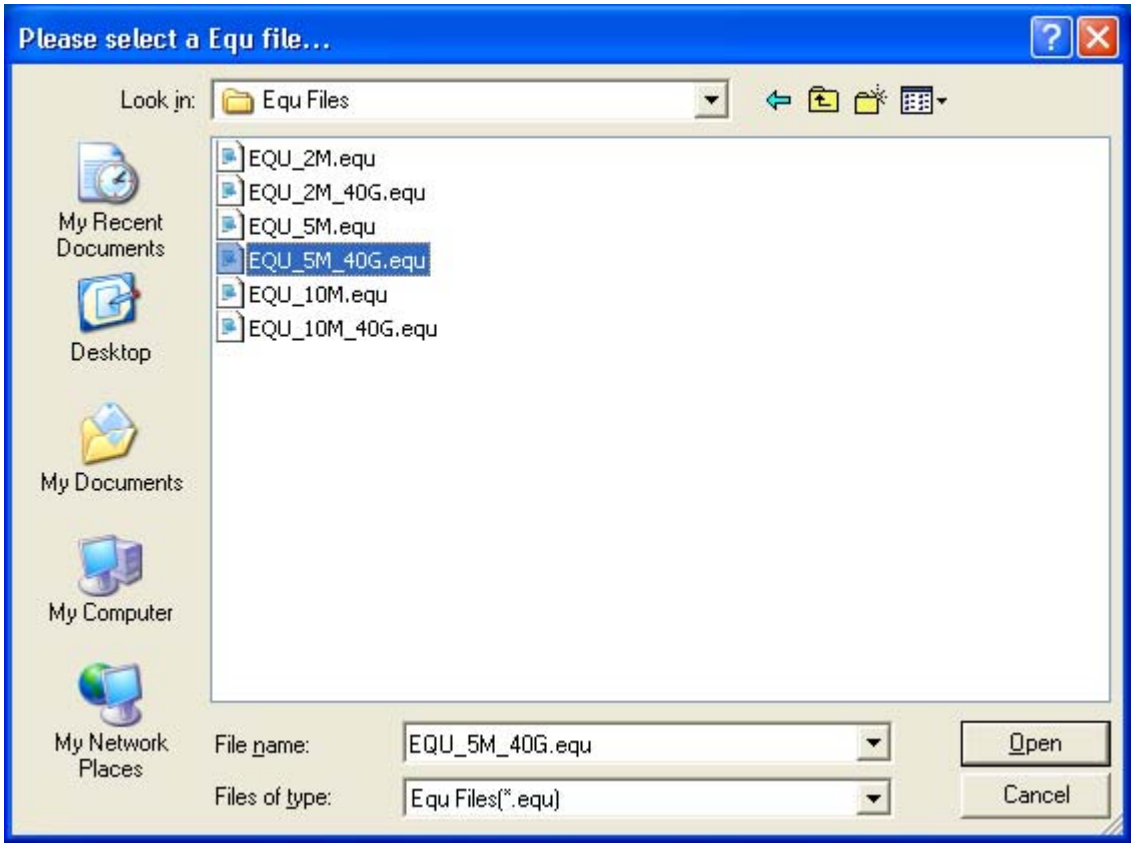

Figure 70 Selecting User Defined File

10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

Table 29 Non-ISI Jitter at Internal and Compliance Points.

	Receiver package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.339 UI	0.330 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.465 UI	0.442 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.1*.

23
Cable Eye Diagram Tests

This section provides the guidelines for cable eye diagram tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Cable Eye Diagram Tests

When performing the cable eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 71 and Figure 72 show a physical connection for making differential and single-ended connections.

.

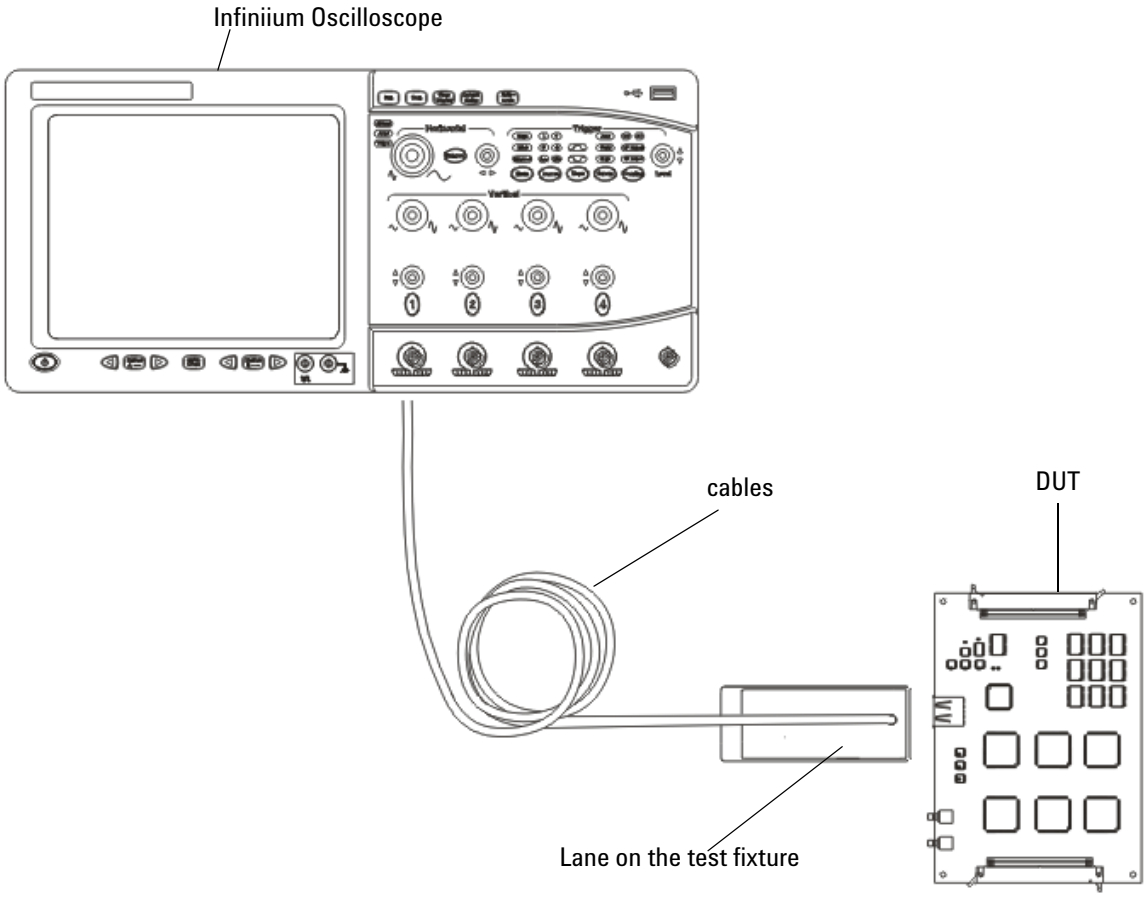

Figure 71 Probing for Differential Tests - Cable Eye Diagram Tests (Single Connection with DisplayPort Test Fixture)

.

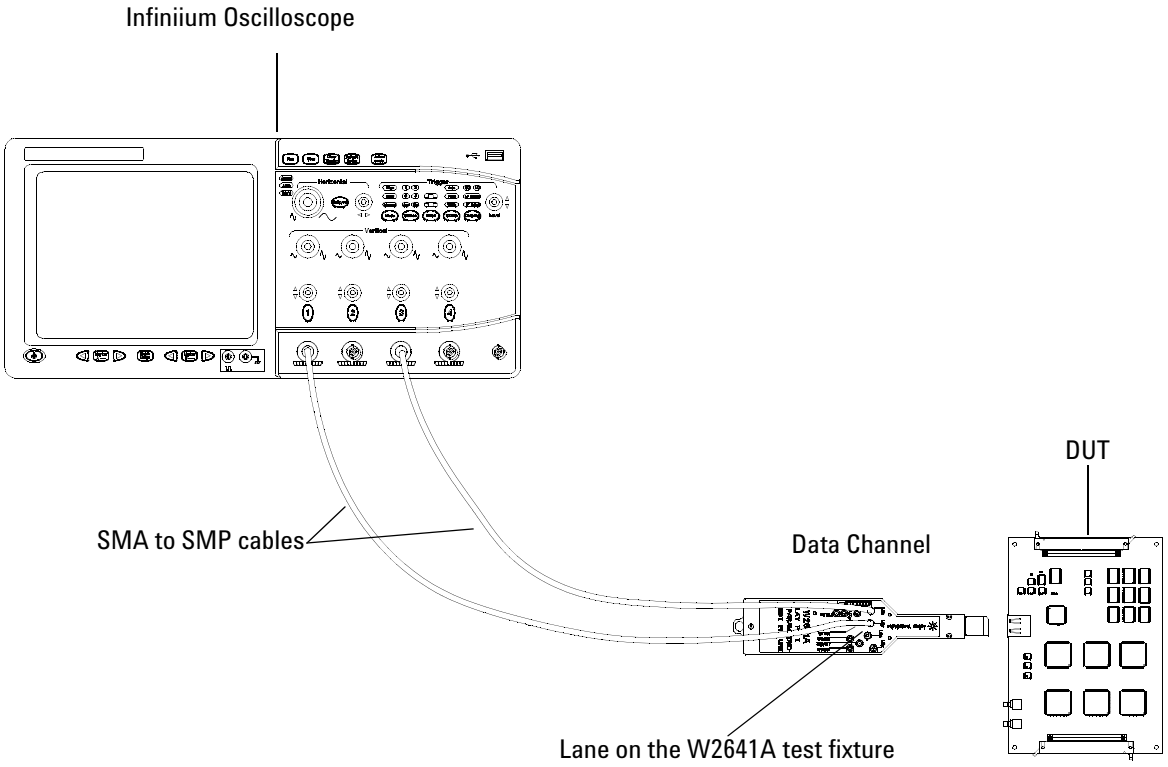

Figure 72 Differential Measurement Setup Using Two Single Ended Connections - Cable Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see Chapter 30, “InfiniiMax Probing,” starting on page 299.

Cable Eye Diagram Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in transmitted data. The test must use a PRBS 7 test pattern at all voltage levels. The test should be performed without pre-Emphasis.

The cable eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Eye Diagram Test - Lane # - Cable Eye Diagram Test where # is the lane number to be tested.

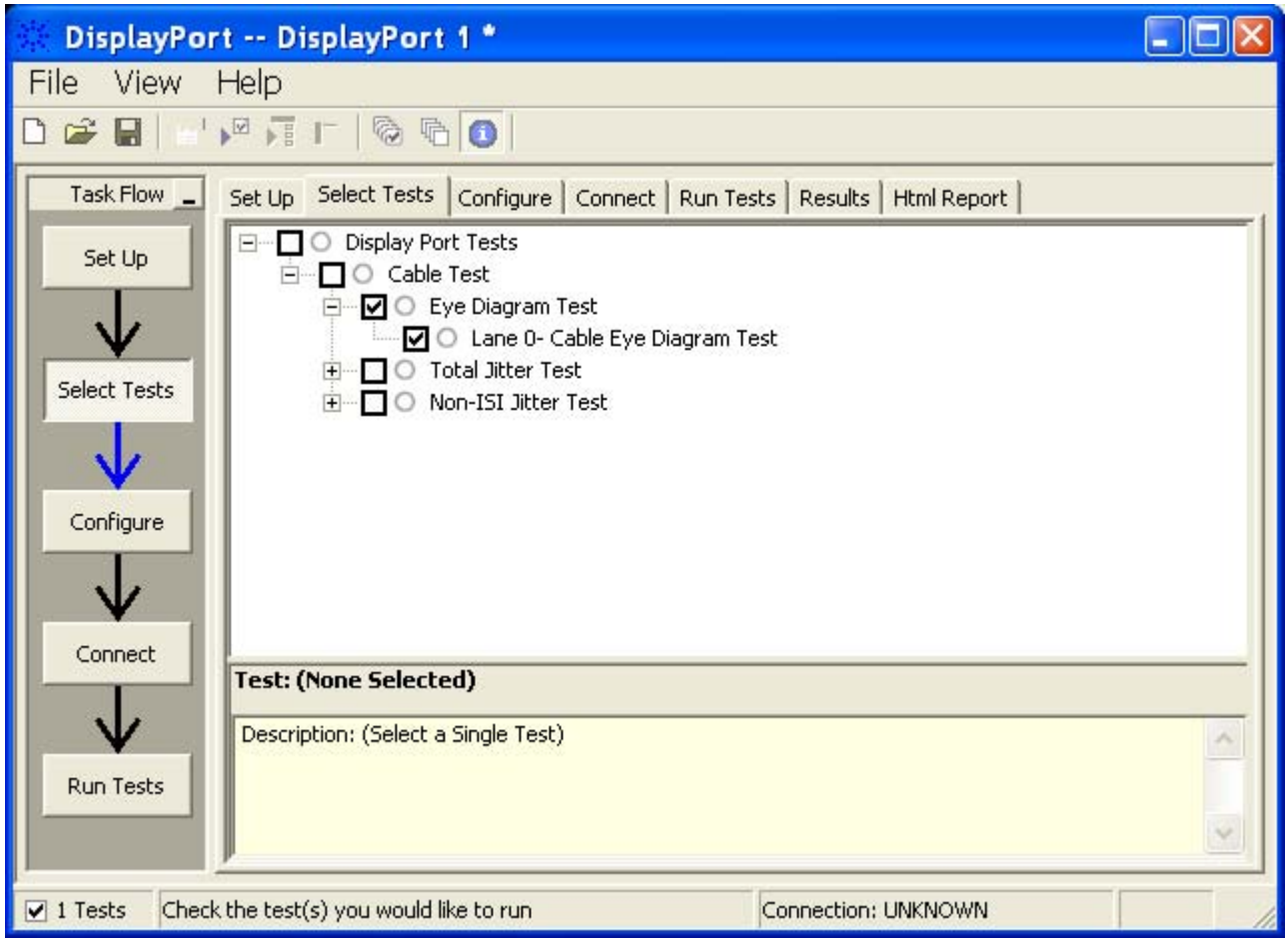

Figure 73 Selecting Cable Eye Diagram Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 30), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 30 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.

Table 30 Test Configuration Options

Configuration Option	Description
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

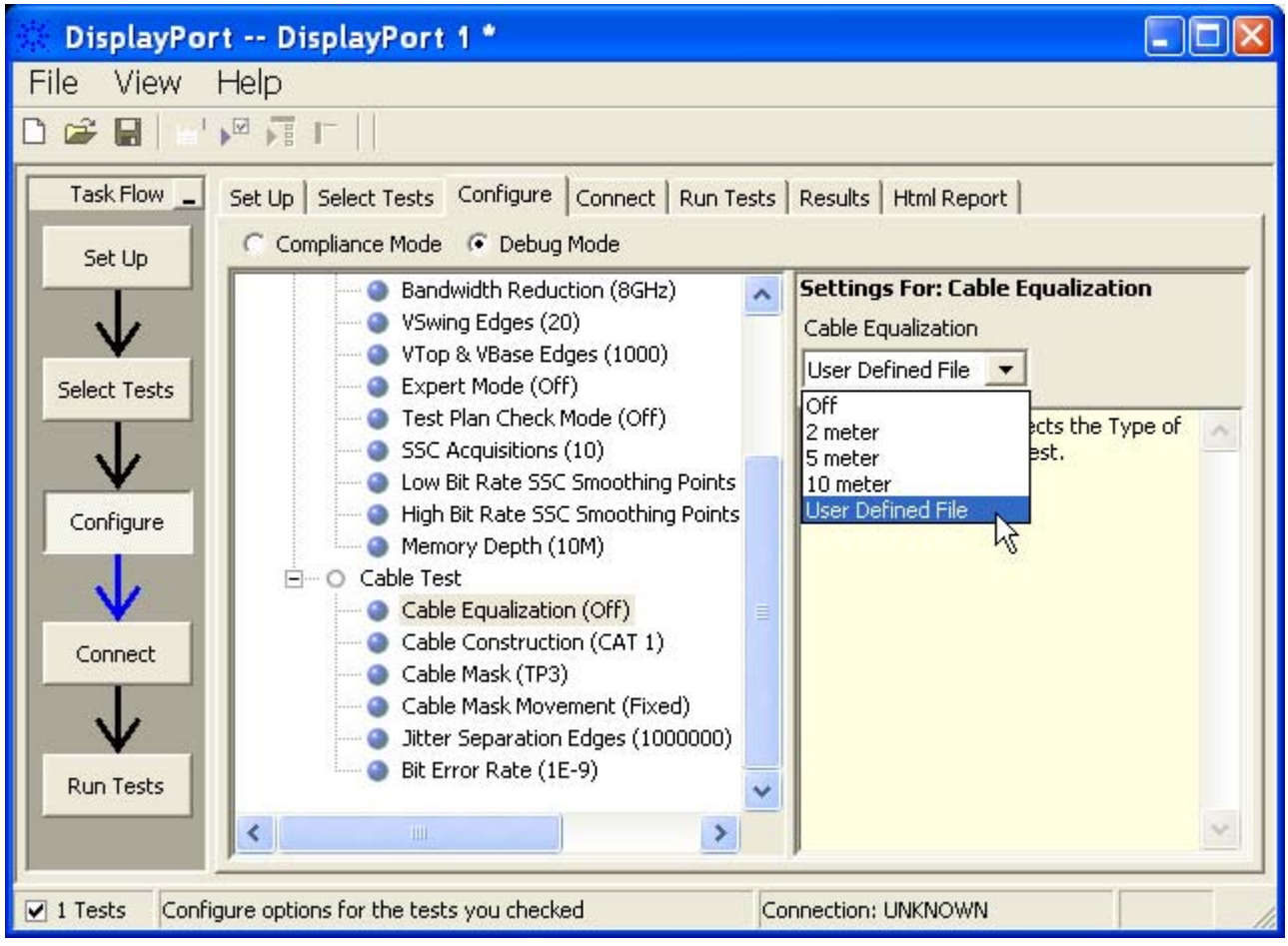

Figure 74 Selecting User Defined File for the Cable Equalizer

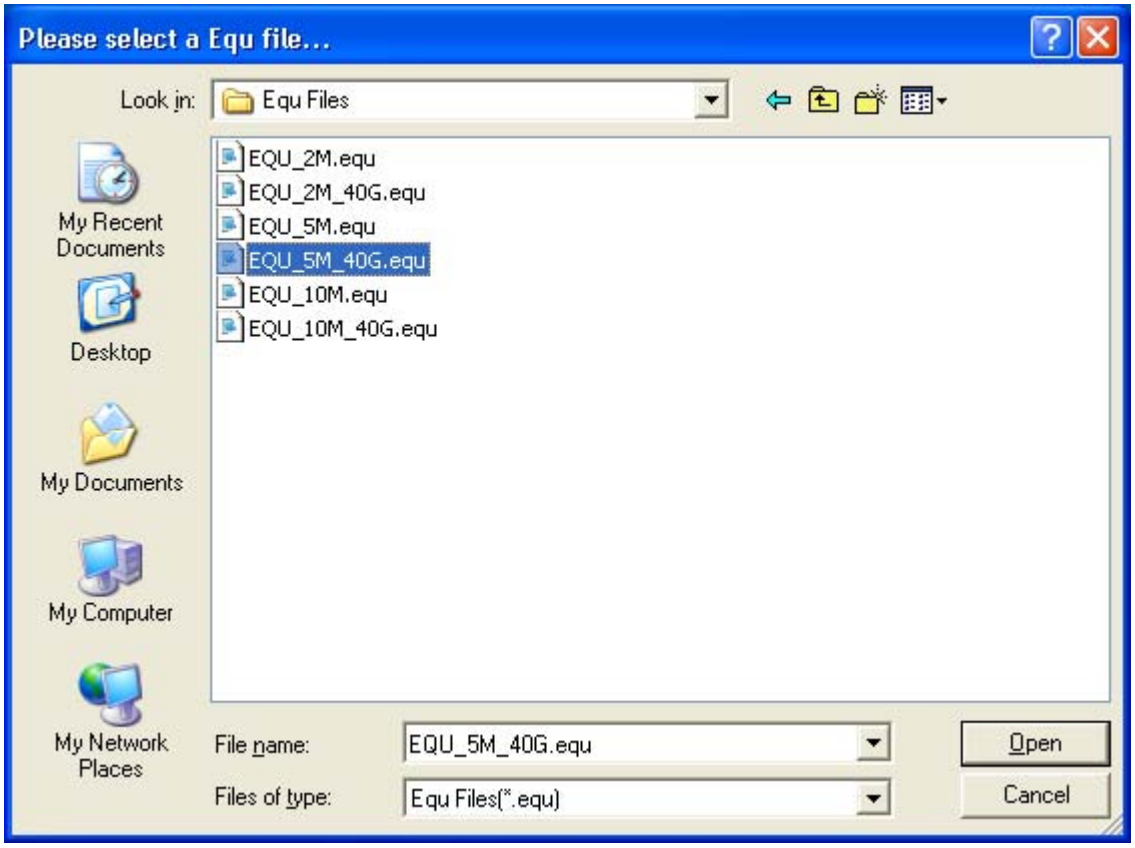

Figure 75 Selecting User Defined File

10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 31 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 31 Cable Eye Vertices for TP3

	Bit Rate	
Mask Point	**Reduced (1.6 Gb/s)**	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

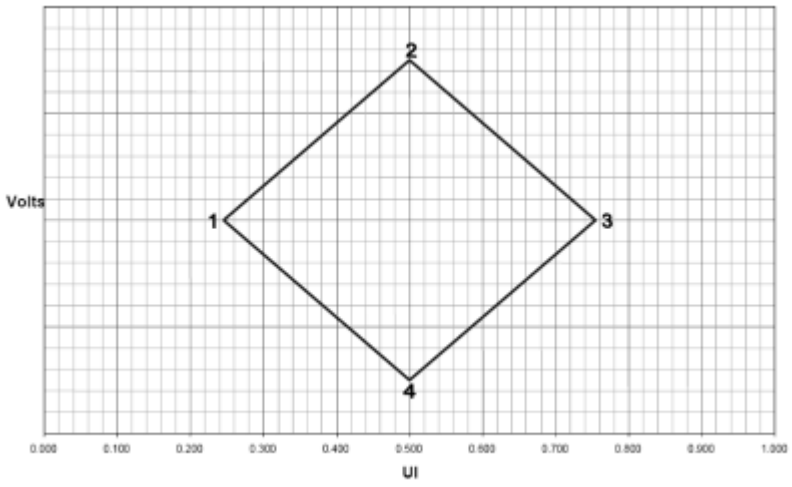

Figure 76 The Cable Eye Mask at TP3

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.*

23 Cable Eye Diagram Tests

24
Cable Total Jitter Tests

This section provides the guidelines for cable total jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Cable Total Jitter Tests

When performing the cable total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 77 and Figure 78 show a physical connection for making differential and single-ended connections.

.

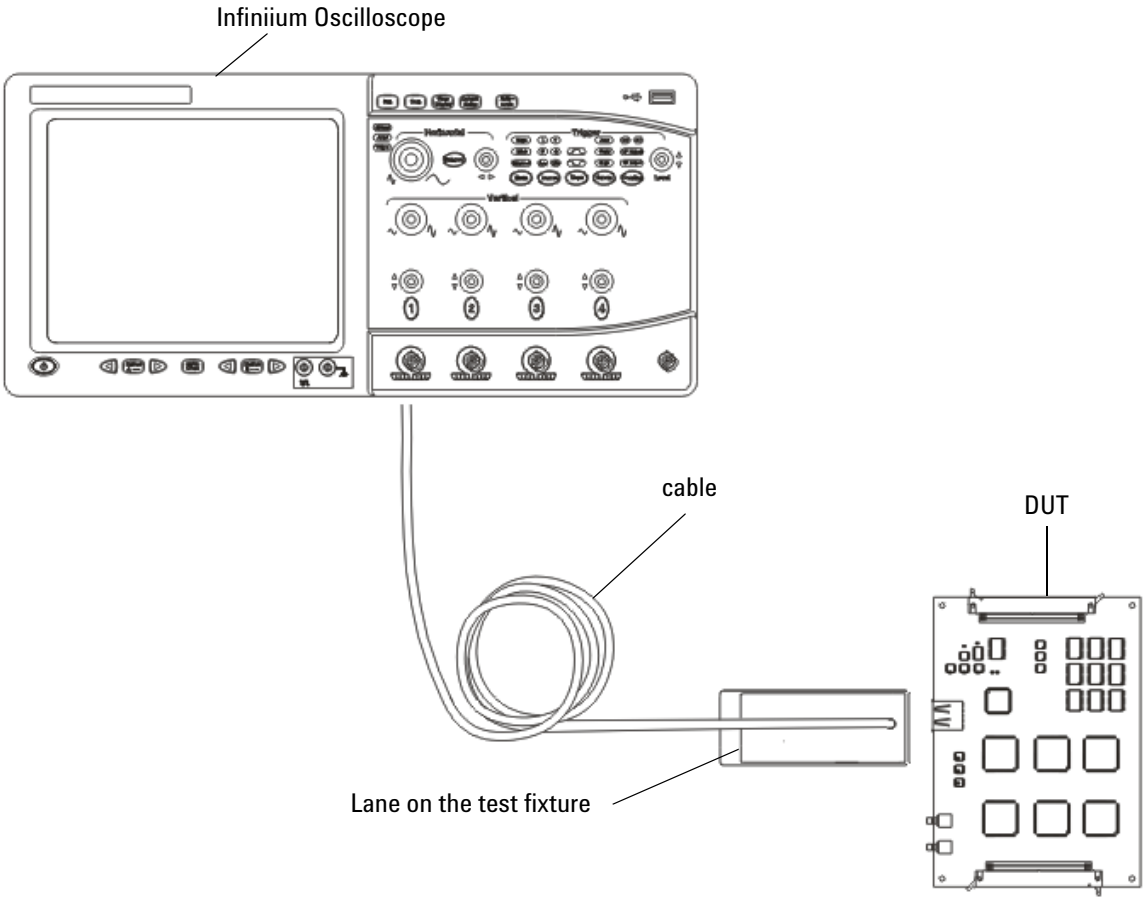

Figure 77 Probing for Differential Tests - Cable Total Jitter Tests (Single Connection with DisplayPort Test Fixture)

.

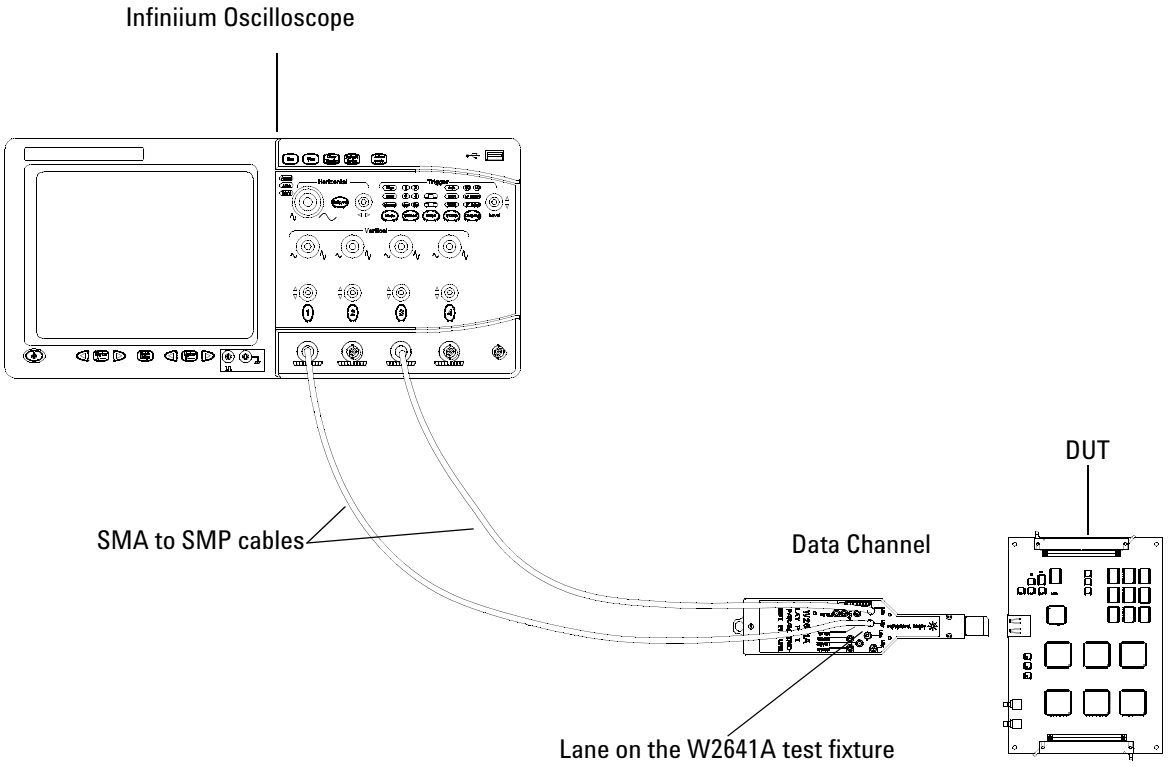

Figure 78 Differential Measurement Setup Using Two Single Ended Connections - Cable Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Cable Total Jitter Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Total Jitter Test - Lane # - Cable Total Jitter Test where # is the lane number to be tested.

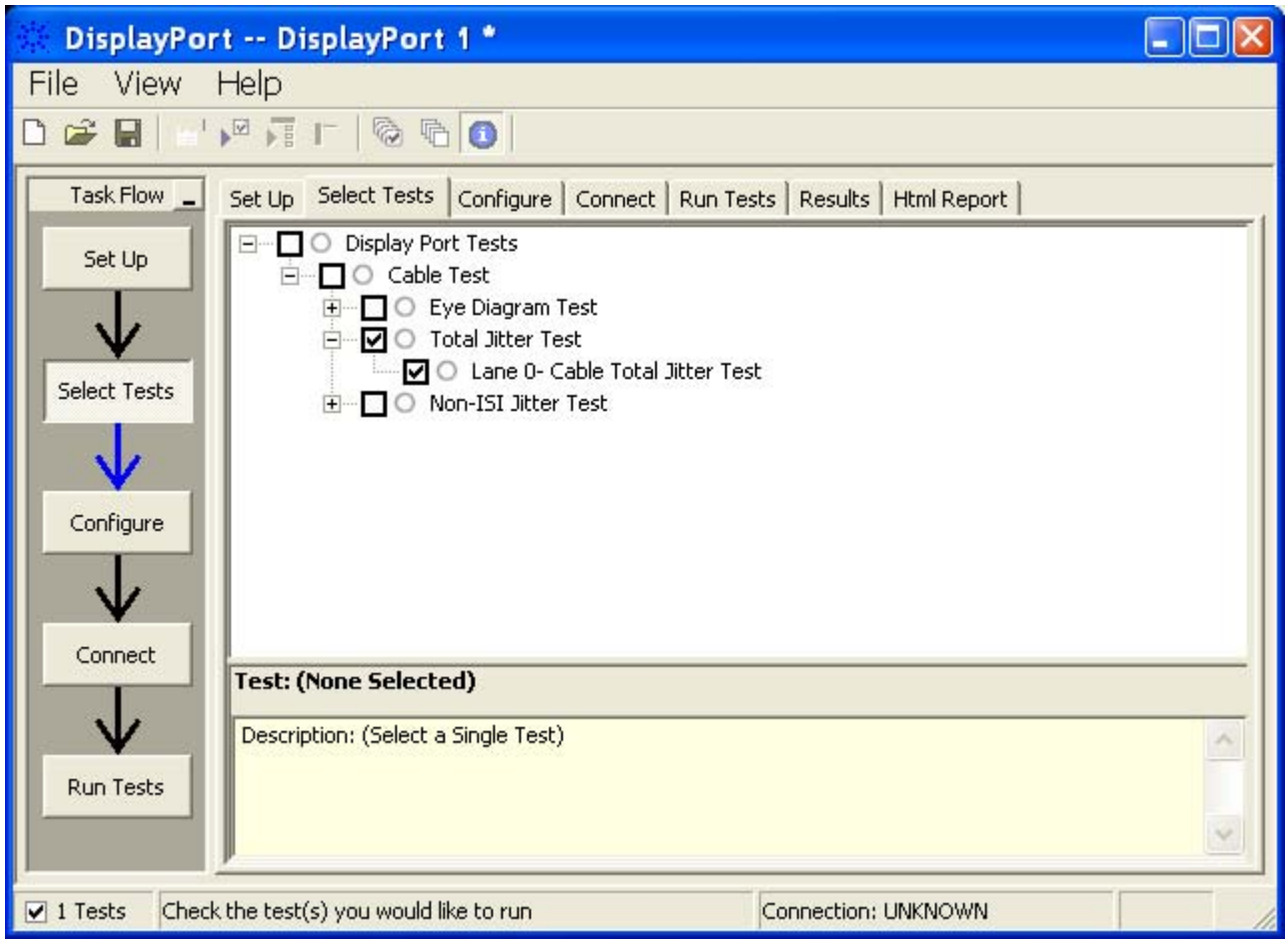

Figure 79 Selecting Cable Total Jitter Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 32), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 32 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.

Table 32 Test Configuration Options

Configuration Option	Description
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

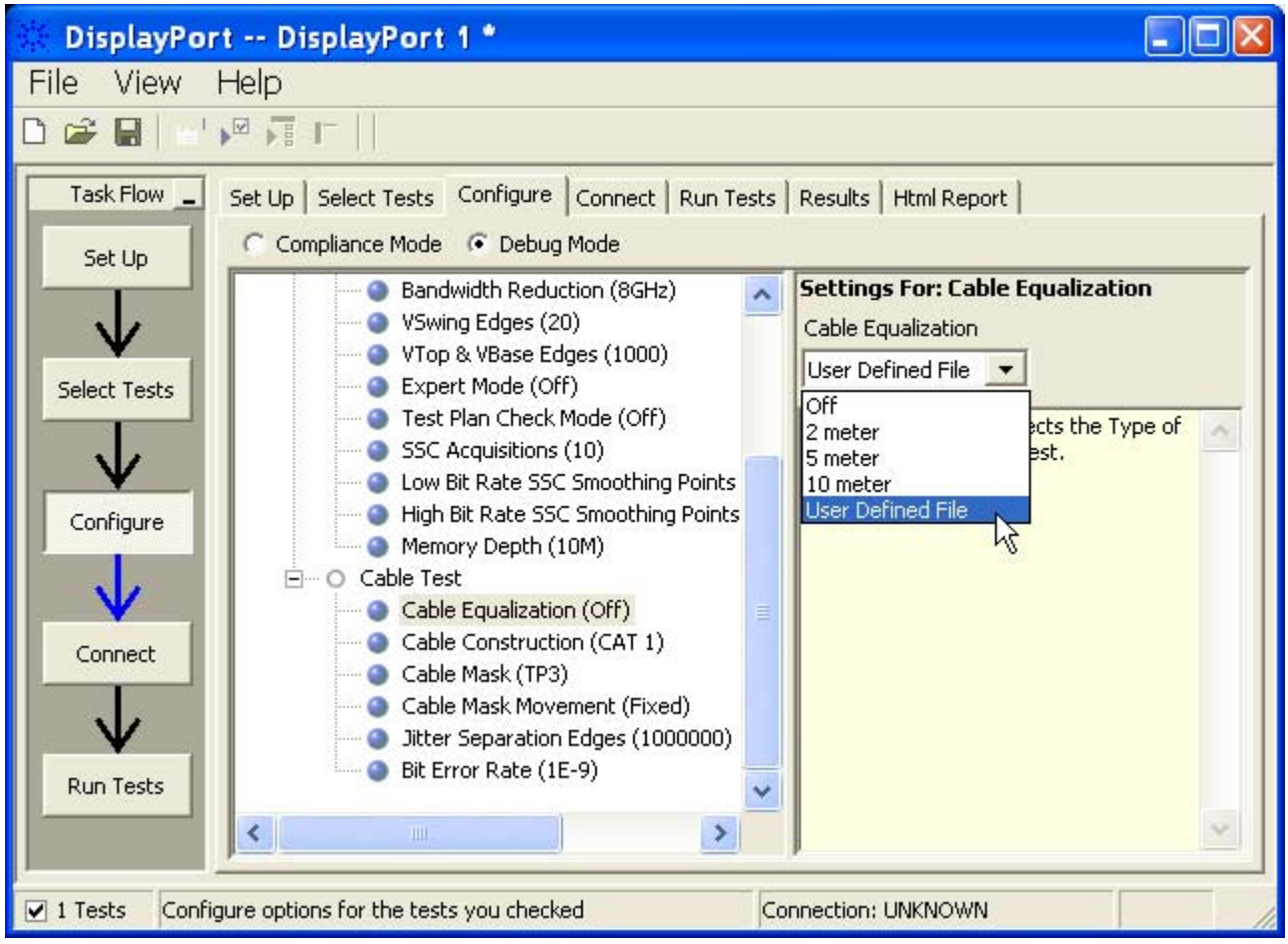

Figure 80 Selecting User Defined File for the Cable Equalizer

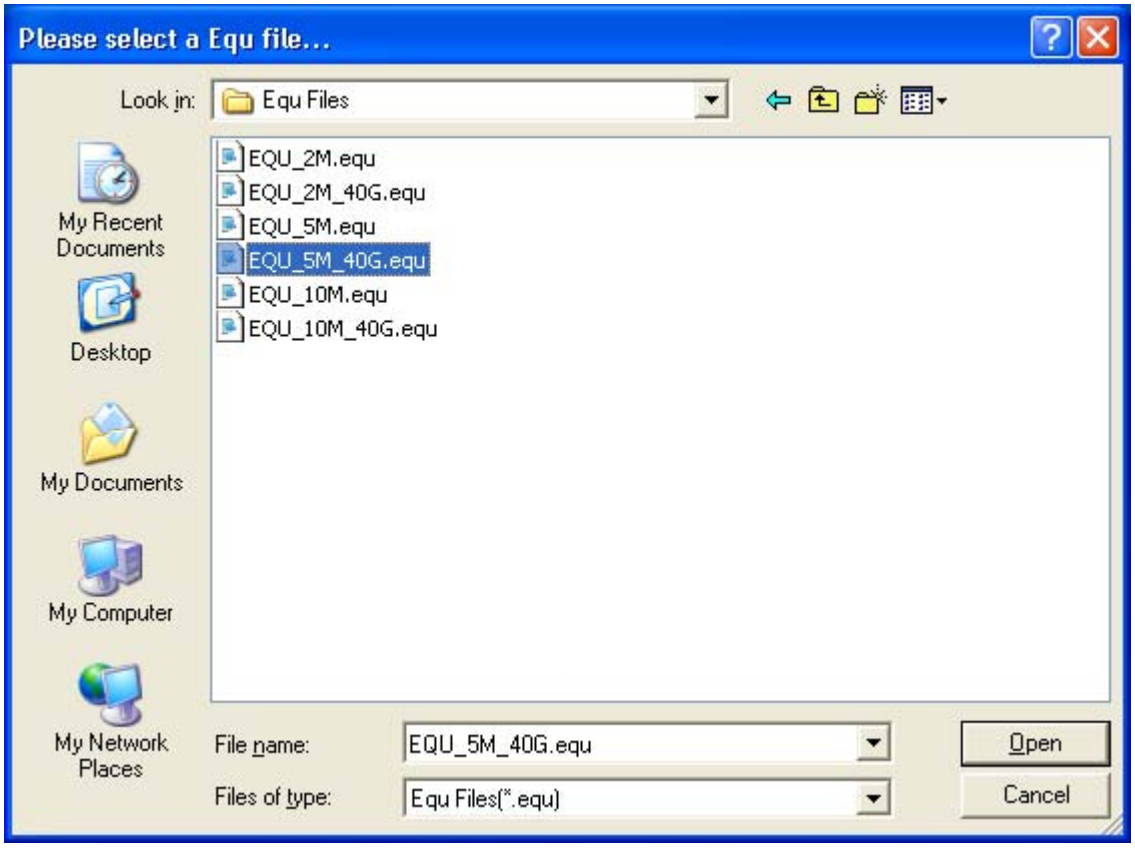

Figure 81 Selecting User Defined File

10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

-

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.*

25
Cable Non-ISI Jitter Tests

This section provides the guidelines for cable non-ISI jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Cable Non-ISI Jitter Tests

When performing the cable non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 82 and Figure 83 show a physical connection for making differential and single-ended connections.

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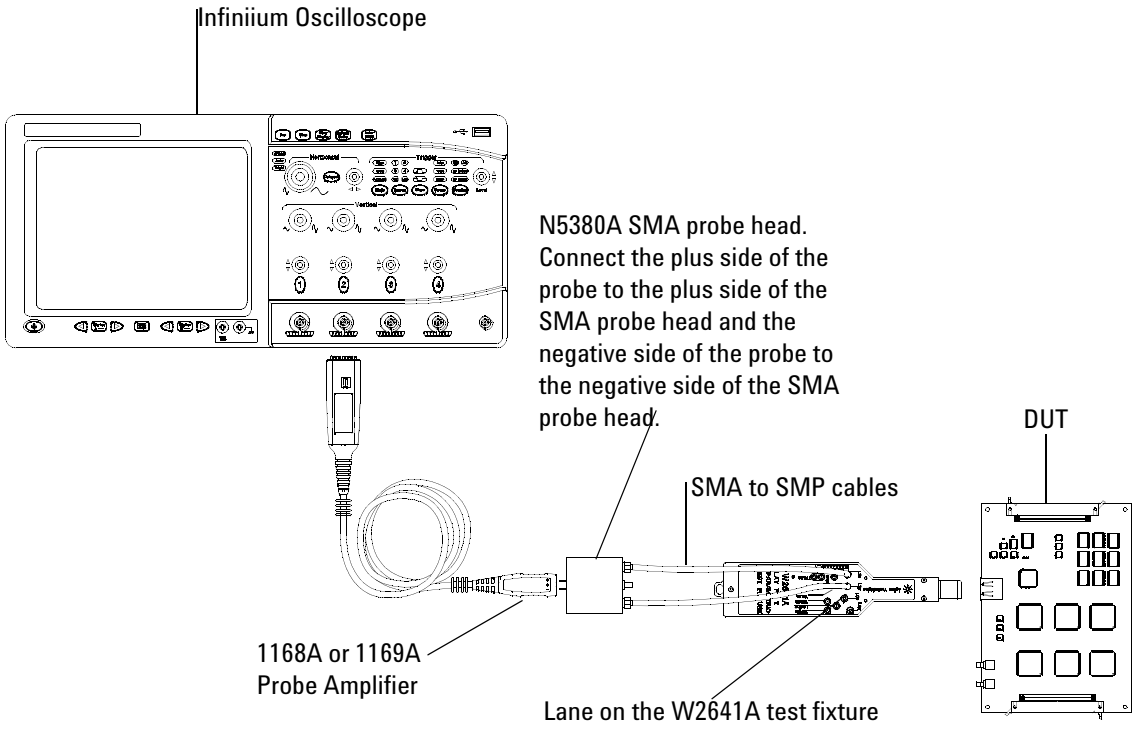

Figure 82 Probing for Differential Tests -Cable Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

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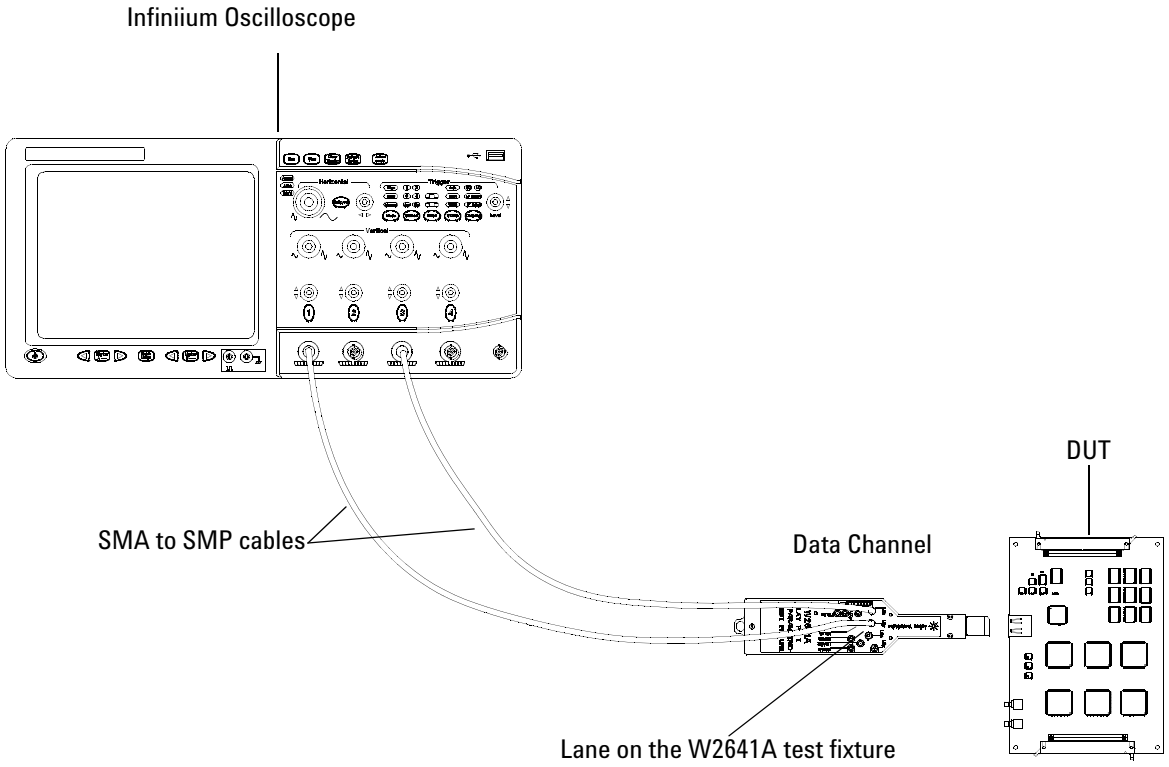


Figure 83 Differential Measurement Setup Using Two Single Ended Connections - Cable Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Cable Non-ISI Jitter Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.
2. Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the Device ID, Operator ID, Project ID, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Non-ISI Jitter - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

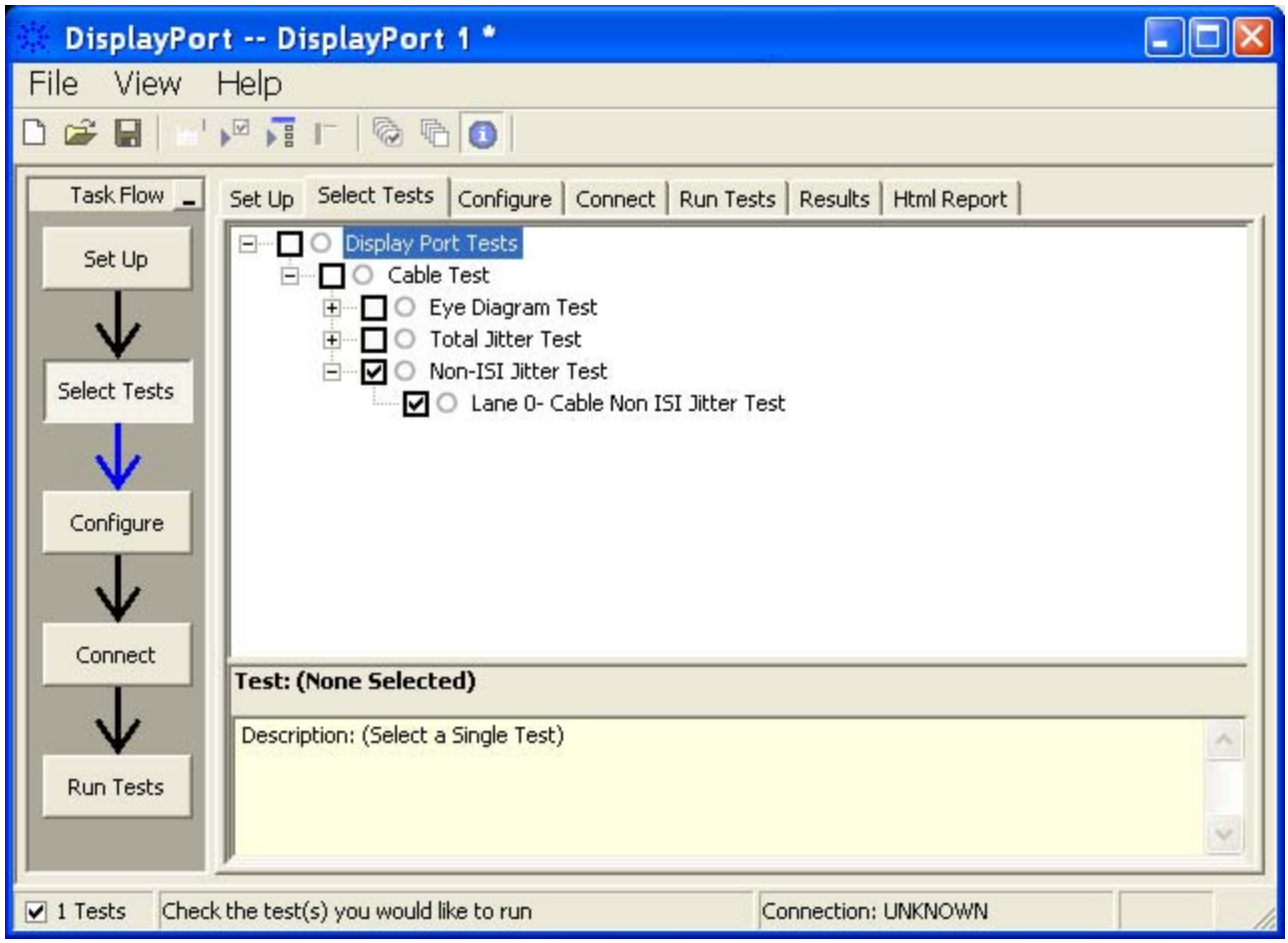


Figure 84 Selecting Cable Non-ISI Jitter Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 33), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 33 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.

Table 33 Test Configuration Options

Configuration Option	Description
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

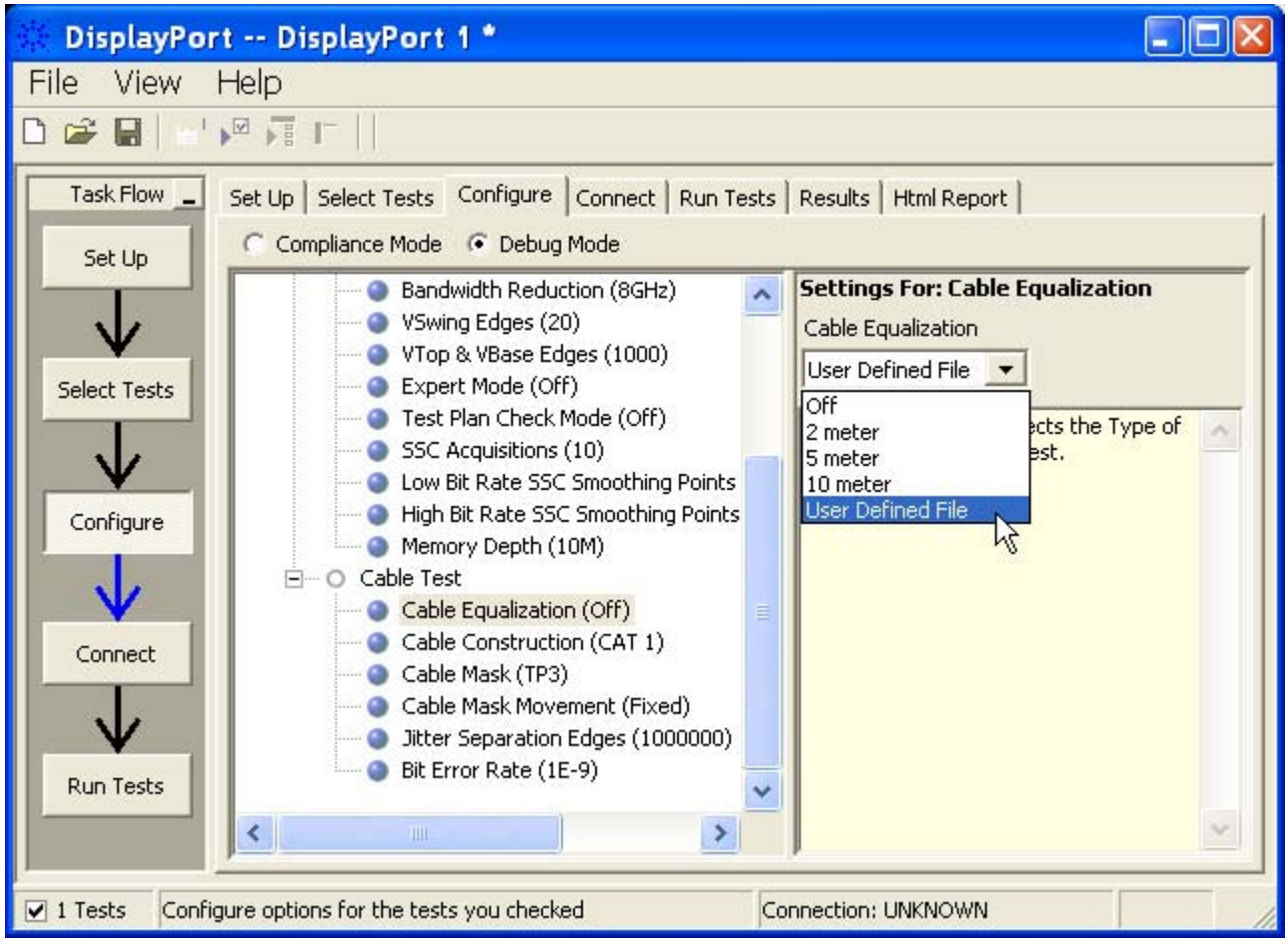


Figure 85 Selecting User Defined File for the Cable Equalizer

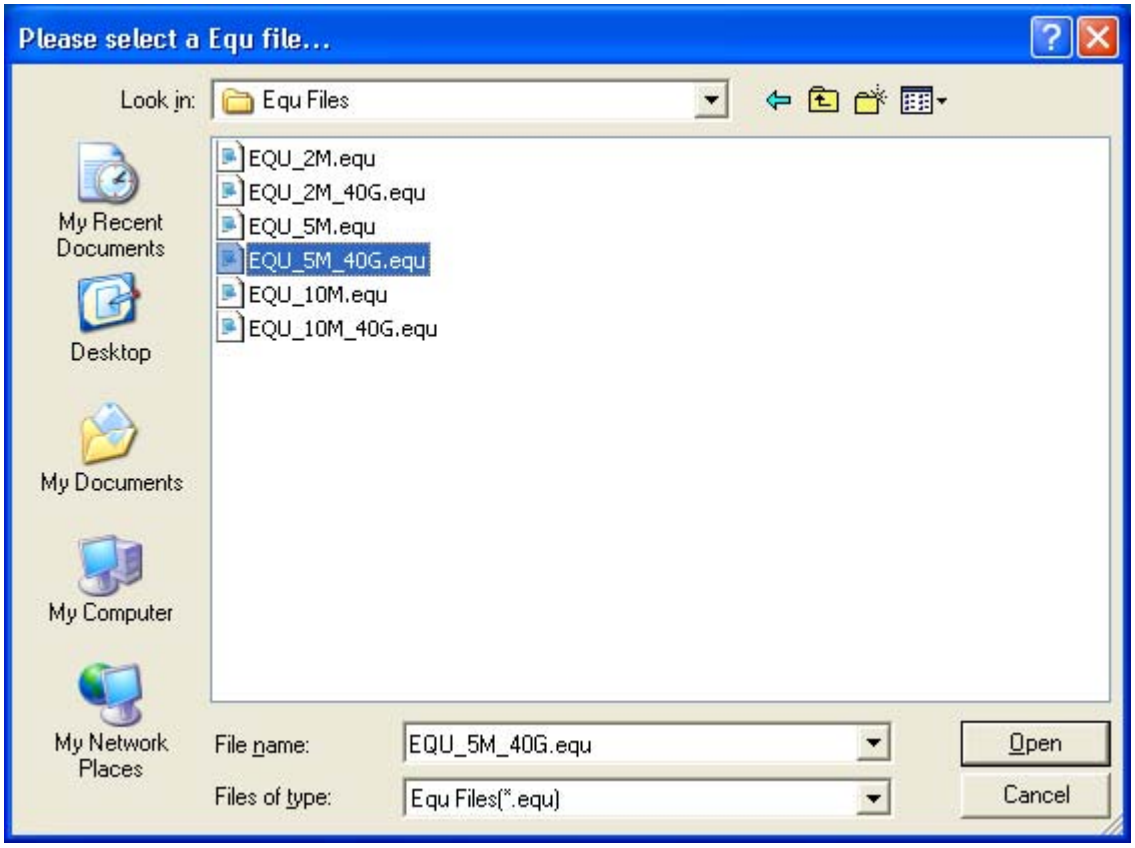


Figure 86 Selecting User Defined File

The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file

PASS Condition

Table 34 Non-ISI Jitter at Internal and Compliance Points.

	Receiver package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.339 UI	0.330 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.465 UI	0.442 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.*

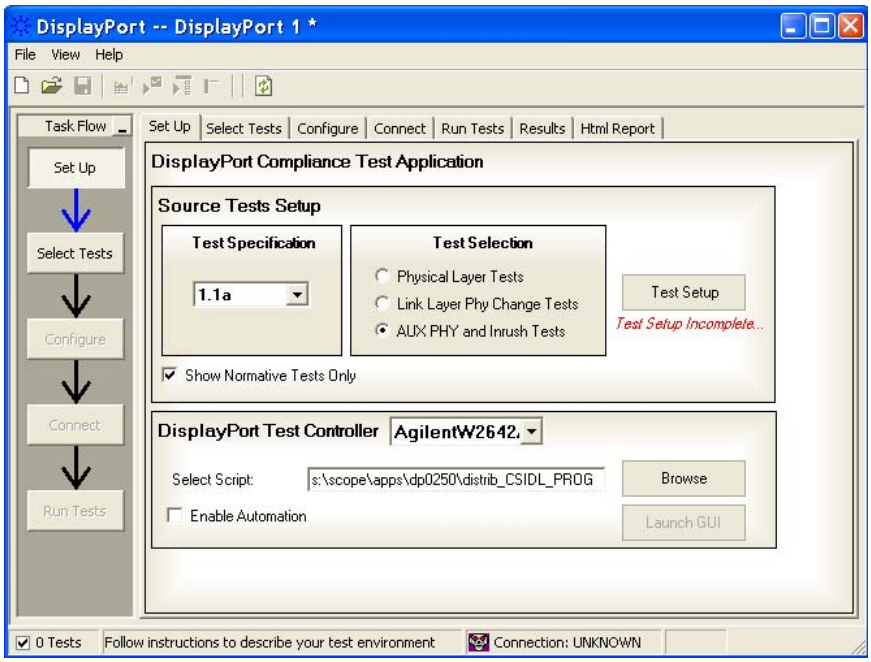
26
Aux Channel Tests

Setting Up for Aux Channel Tests

Before performing the Aux Channel tests, you must go through the set up process.

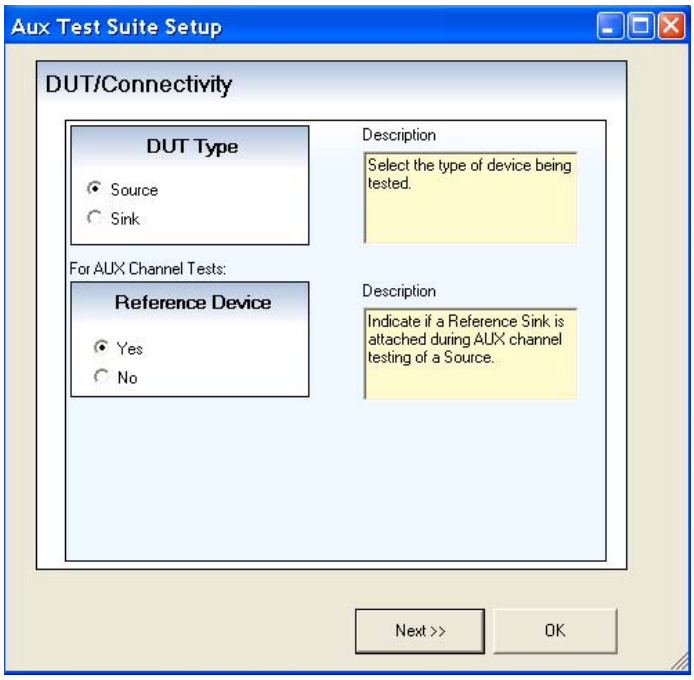
To set up for the Aux Channel tests:

1 On the DisplayPort Compliance application main page, select **AUX PHY and Inrush Tests** in the Test Selection area; then, click the corresponding **Test Setup** button.



2 In the DUT/Connectivity setup page,

a define the device being tested (either a **Source** or a **Sink**).



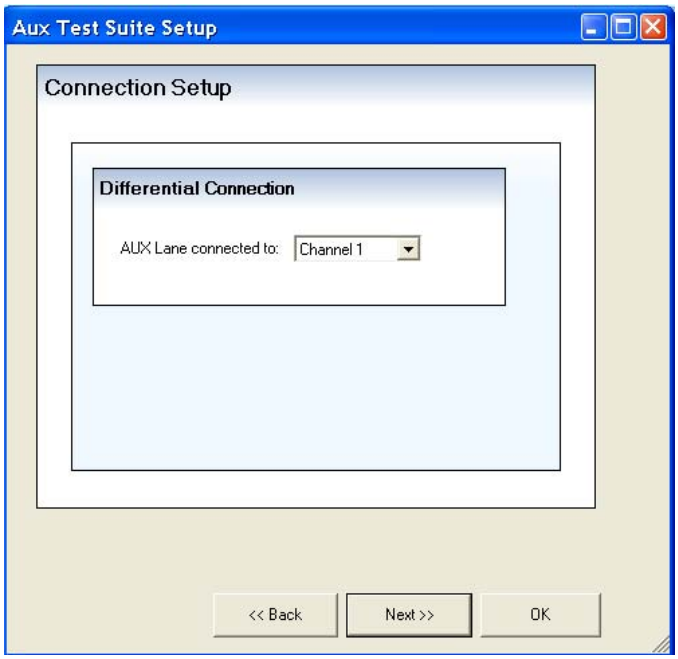
b In the Reference Device area, select either a **Yes** or a **No**. A reference device might be needed to complete Aux transaction between reference device and DUT. This configuration applies to Aux Channel tests only.

Yes – if the reference device is attached during testing. The application expects complete Aux transactions, which consist of at least, a Source Aux command followed by a Sink Aux reply.

No – the application assumes all signals are either a Source or a Sink Aux signal only, depending on the DUT Type selected.

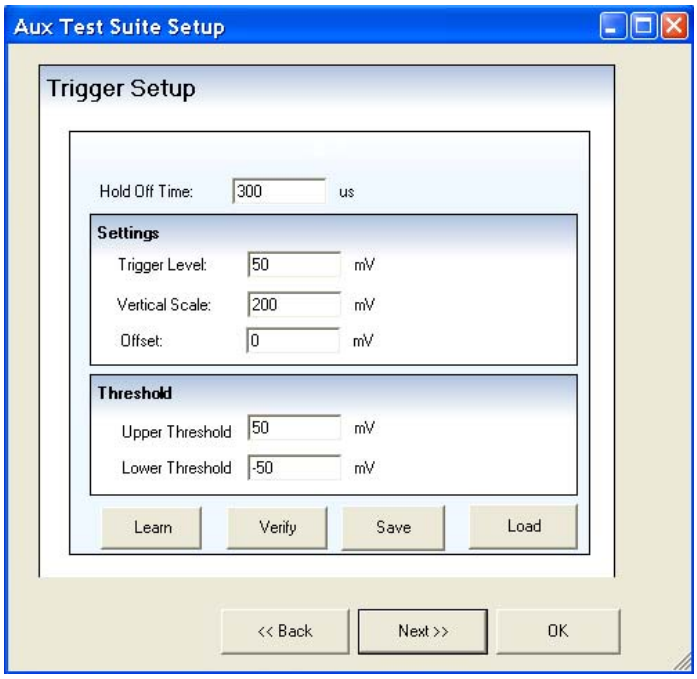
c Click **Next** to go to next page.

3 Next, in the Connection Setup page, select the oscilloscope channel connected to the Aux differential signal.



4 The Trigger Setup page is the most important of all the set up steps because this is the page where you tell the oscilloscope how to trigger on an Aux signal during testing.

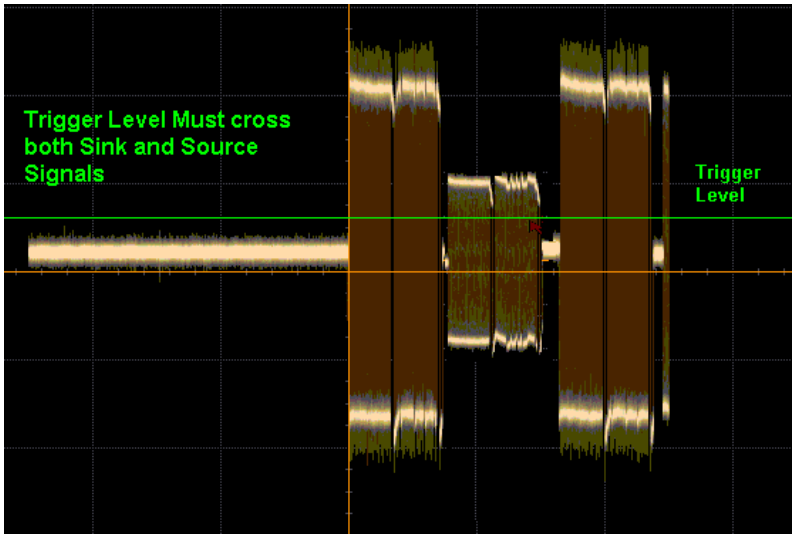
a Descriptions for each parameter are as follows:



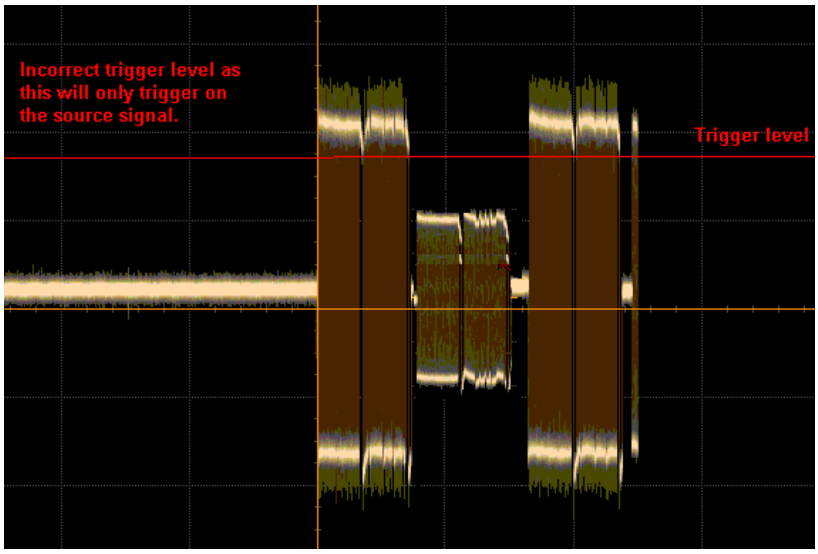
Hold Off Time – the oscilloscope minimum hold off time before triggering the next waveform.

Trigger Level – the Aux channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level so that it is crossing both the Source Command and the Sink Reply signals. For example:

Correct Trigger Level:



Incorrect Trigger Level:

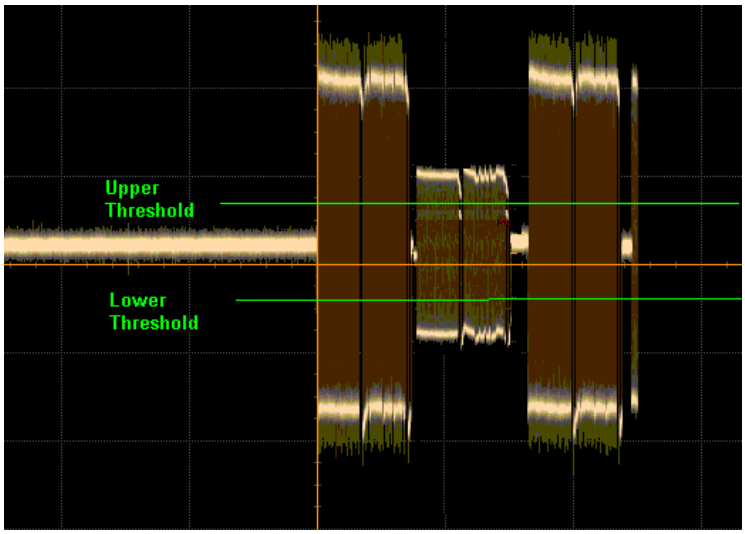


Vertical Scale – the oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope screen.

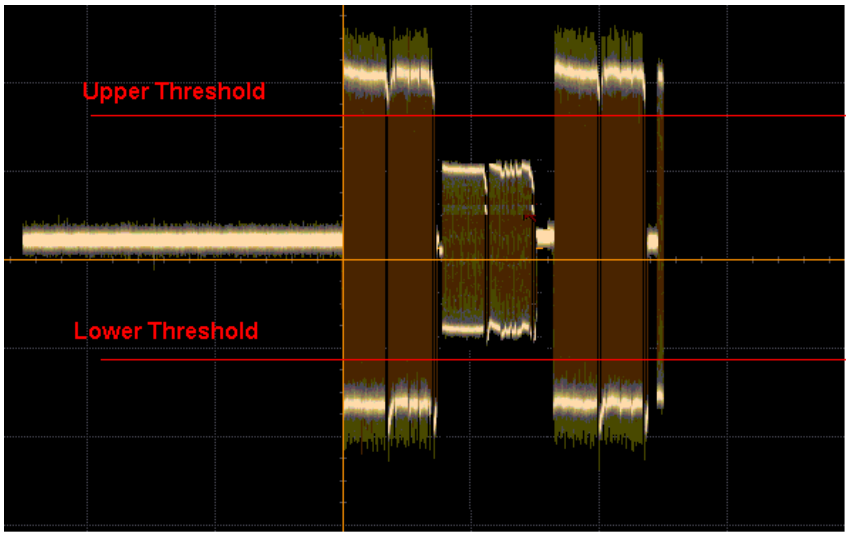
Offset – set the offset so that the center point is aligned with the center of screen.

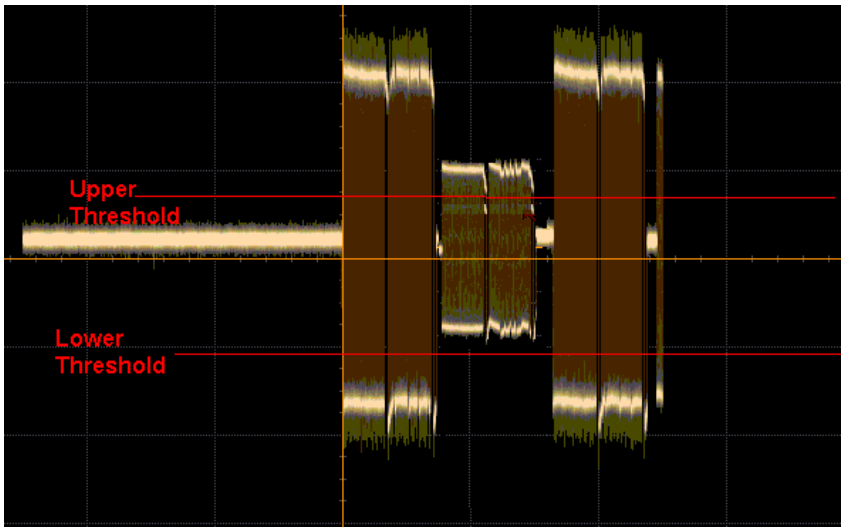
Upper Threshold/Lower Threshold – the threshold level of signal must be set properly so that both upper and lower thresholds are crossing both the Source and the Sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a Source command from a Sink reply. For example:

Threshold correctly set:



Threshold wrongly set:





b In the Trigger Setup page, you can click on the **Learn** button to guide you through getting the trigger setup parameters. However, please note that the learning guide might fail because actual Aux signals from different vendors could vary. We advise you to make sure that the parameters are correctly set as previously described.

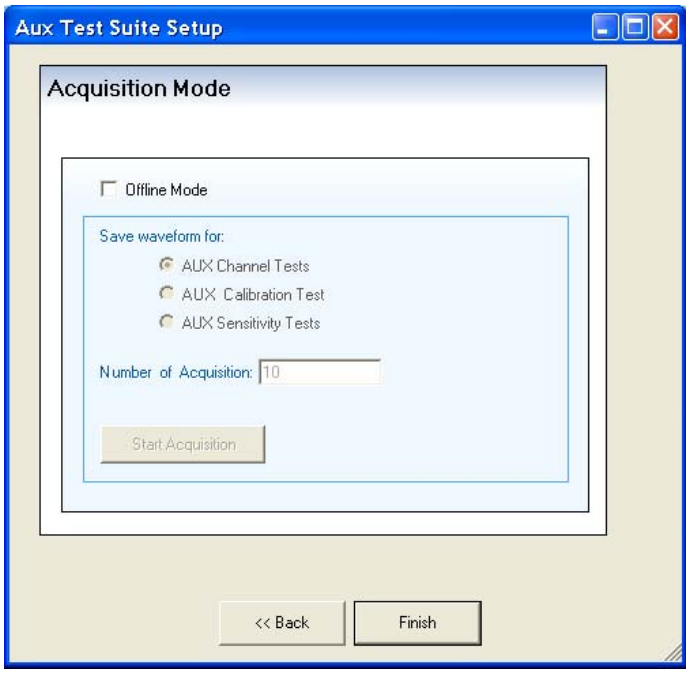
c When done, you can verify the Aux Channel trigger by clicking **Verify** and following the instructions.

d You can **Save** or **Load** the trigger setup configuration as a *.tsf file.

5 Lastly, in the Acquisition Mode page, you can either just finish the setup wizard or enable Offline Mode for debugging purpose.

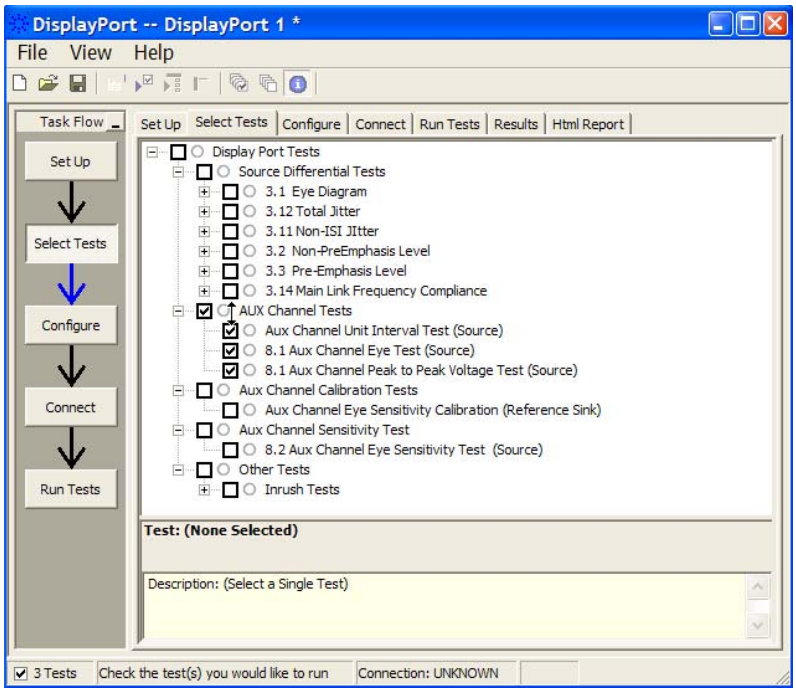
Offline Mode lets you pre-save the waveforms so that you do not need to go through the manual process to initiate Aux transaction during test time.

When Offline Mode is enabled, you can define the number of waveforms to be saved. Select the tests which are meant to use these waveforms after acquisitions. Then, click **Start Acquisition** to start capturing and saving waveforms.



6 Click **Finish** to close the setup wizard.

You are now ready to go to the Select Test tab and select the Aux Channel tests you want to run.



Source Aux Channel Tests

Probing/Connection Setup for Source Aux Channel Tests

When performing the source Aux Channel tests, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

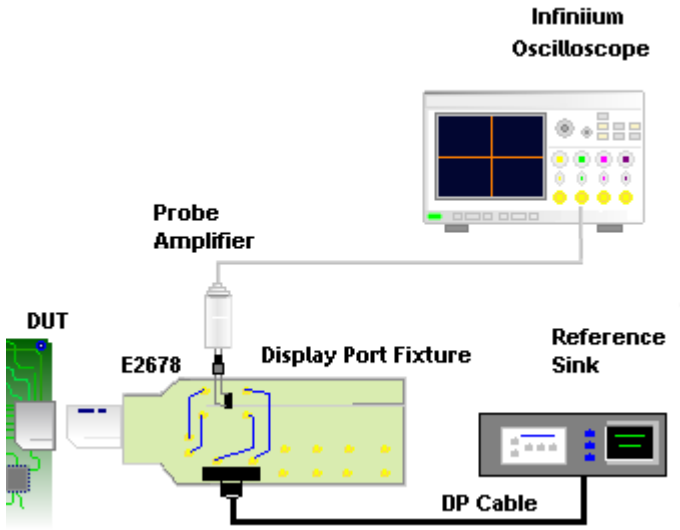


Figure 87 Connection diagram when performing source Aux Channel tests with source DUT connected to a reference sink

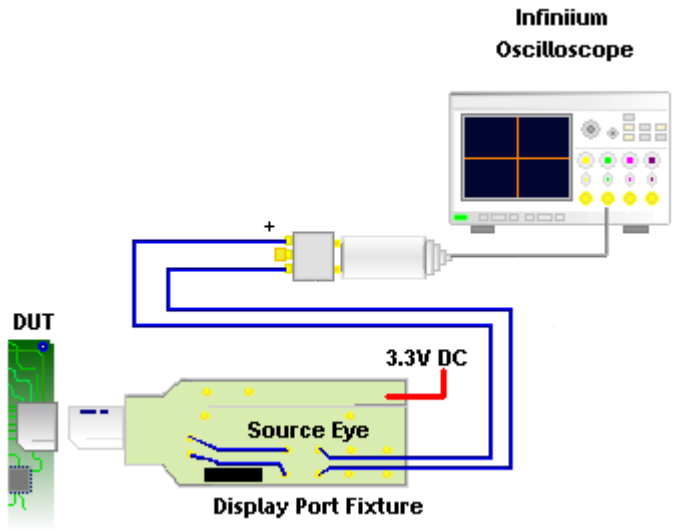


Figure 88 Connection diagram when performing source Aux Channel tests without connecting to a reference sink

Source Aux Channel Unit Interval Test (Informative)

This section provides the guidelines for source Aux channel unit interval test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate the Aux channel unit interval of a DisplayPort source device.

Test Procedure

1 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in "Setting Up for Aux Channel Tests" on page 224.

3 If reference sink is connected:

   a Connect **Ap**(Sink AUX+) & **An**(Sink AUX-) to Port **p & n** of the "**AUX Sensitivity Sink**" section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the "**AUX Sensitivity Source**" section of the W2641B fixture.

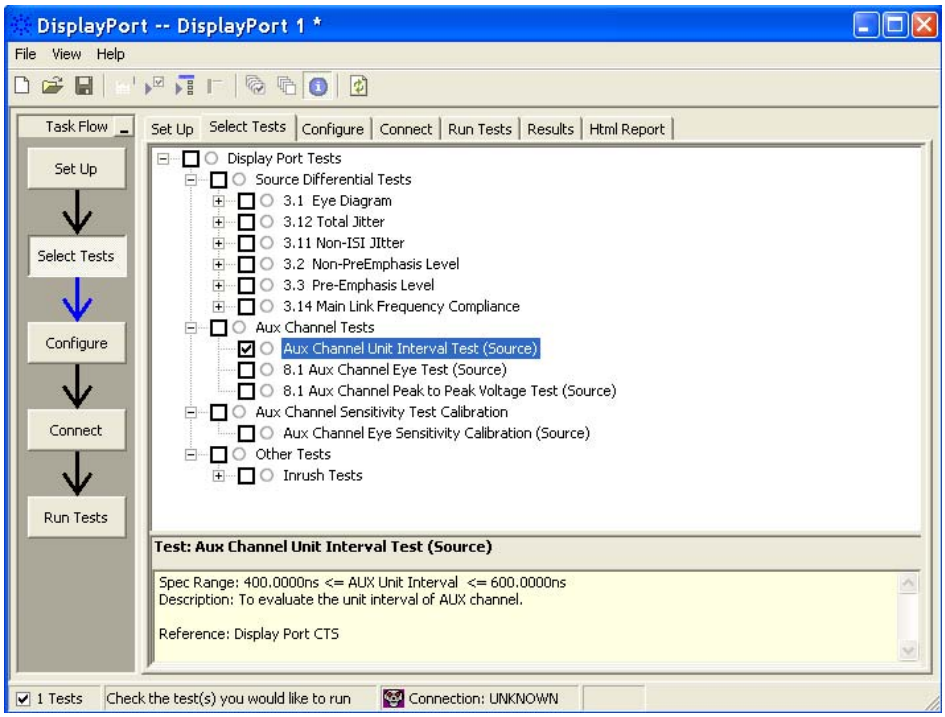
   c Connect probe from W2641B to an oscilloscope channel.

If reference sink is not connected:

a Connect port **AUXp** & **AUXn** of fixture to the "**To Source**" port labeled in the "**Source Eye**" section of fixture W2641B.

b Connect port **p & n** in the "**Source Eye to Scope**" section in fixture W2641B.

4 Go to "Select Tests" tab of compliance application. Navigate to "Aux Channel Unit Interval Test (Source)".



5 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

400 ns ≤ AUX Unit Interval ≤ 600 ns.

Source Aux Channel Eye Test (Normative)

This section provides the guidelines for source Aux channel eye test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate Aux channel to ensure that the timing and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.

Test Procedure

1 Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in “Setting Up for Aux Channel Tests" on page 224.

3 If reference sink is connected:

   a Connect **Ap**(Sink AUX+) & **An**(Sink AUX-) to Port **p & n** of the “**AUX Sensitivity Sink**” section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the “**AUX Sensitivity Source**” section of the W2641B fixture.

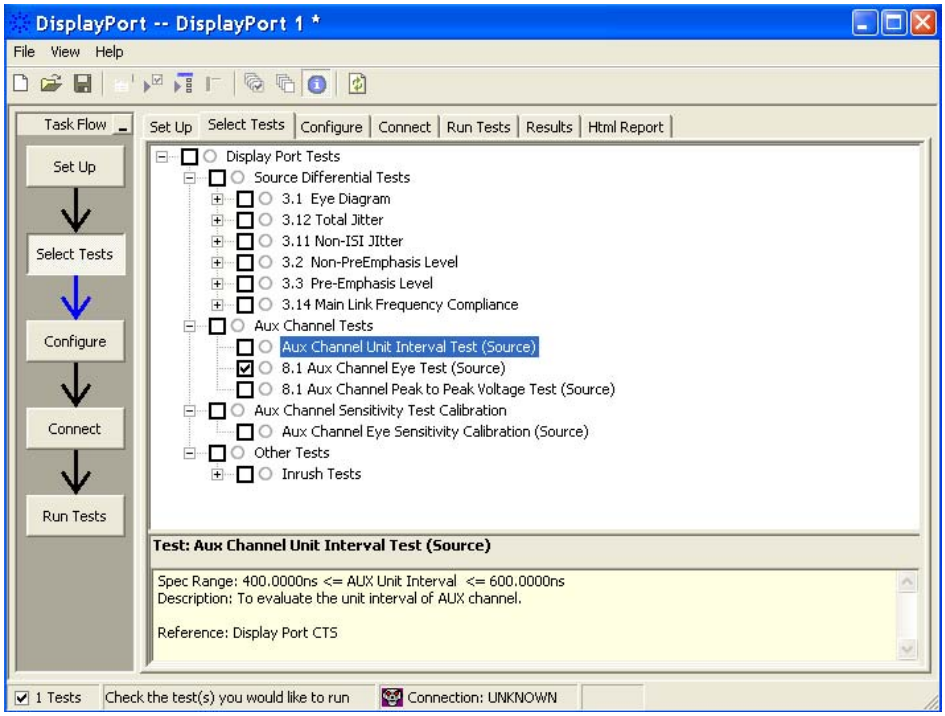
   c Connect probe from W2641B to an oscilloscope channel.

   If reference sink is not connected:

   a Connect port **AUXp** & **AUXn** of fixture to the “To Source” port labeled in the “**Source Eye**” section of fixture W2641B.

   b Connect port **p & n** in the “**Source Eye to Scope**” section in fixture W2641B.

4 Go to “Select Tests” tab of compliance application. Navigate to “8.1 Aux Channel Eye Test (Source)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

Mask Point	Coordinates
1	0.13, 0
2	0.23, 0.145
3	0.77, 0.145
4	0.86, 0
5	0.77, -0.145
6	0.23, -0.145

Mask Test: Zero mask failures.

Source Aux Channel Peak-to-Peak Voltage Test (Normative)

This section provides the guidelines for source Aux channel peak-to-peak voltage test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate the Aux channel peak-to-peak voltage of a DisplayPort system.

Test Procedure

1 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux channel test procedures and parameters as shown in "Setting Up for Aux Channel Tests" on page 224.

3 If reference sink is connected:

   a Connect **Ap**(Sink AUX+) & **An**(Sink AUX-) to Port **p & n** of the "**AUX Sensitivity Sink**" section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the "**AUX Sensitivity Source**" section of the W2641B fixture.

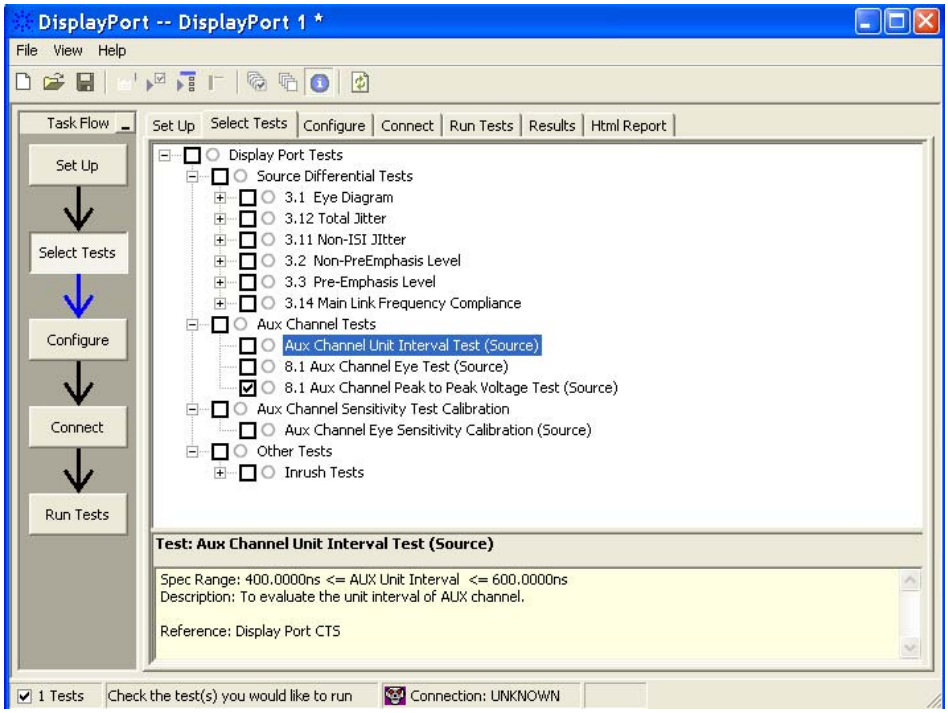
   c Connect probe from W2641B to an oscilloscope channel.

   If reference sink is not connected:

   a Connect port **AUXp** & **AUXn** of fixture to the "**To Source**" port labeled in the "**Source Eye**" section of fixture W2641B.

   b Connect port **p & n** in the "**Source Eye to Scope**" section in fixture W2641B.

4 Go to “Select Tests” tab of compliance application. Navigate to “8.1 Aux Channel Peak-to-Peak Voltage Test (Source)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

Vpp(Source) > 290 mV.

Sink Aux Channel Tests

Probing/Connection Setup for Sink Aux Channel Tests

When performing the sink Aux channel tests, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

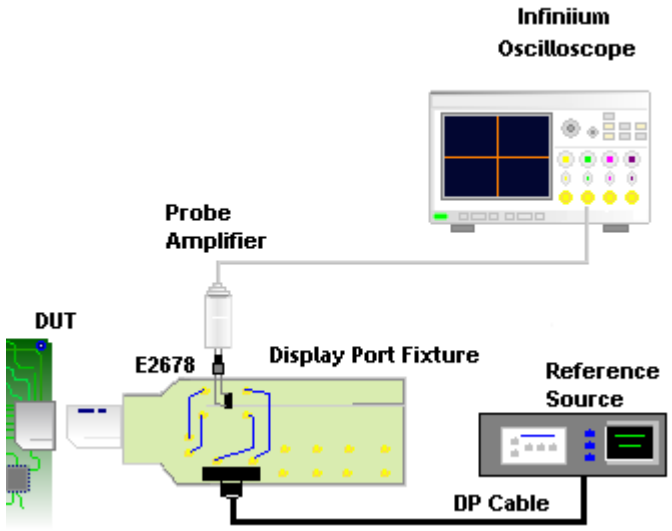


Figure 89 Connection diagram when performing sink Aux channel tests with sink DUT connected to a reference source

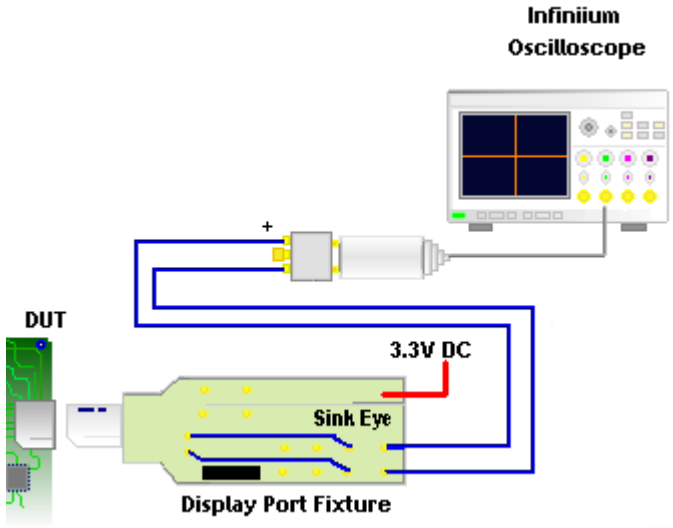


Figure 90 Connection diagram when performing sink Aux channel tests without connecting to a reference source

Sink Aux Channel Unit Interval Test (Informative)

This section provides the guidelines for sink Aux channel unit interval test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate the Aux channel unit interval of a DisplayPort sink device.

Test Procedure

1 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in "Setting Up for Aux Channel Tests" on page 224.

3 If reference source is connected:

   a Connect **Ap**(Source AUX+) & **An**(Source AUX-) to Port **p & n** of the "**AUX Sensitivity Source**" section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the "**AUX Sensitivity Sink**" section of the W2641B fixture.

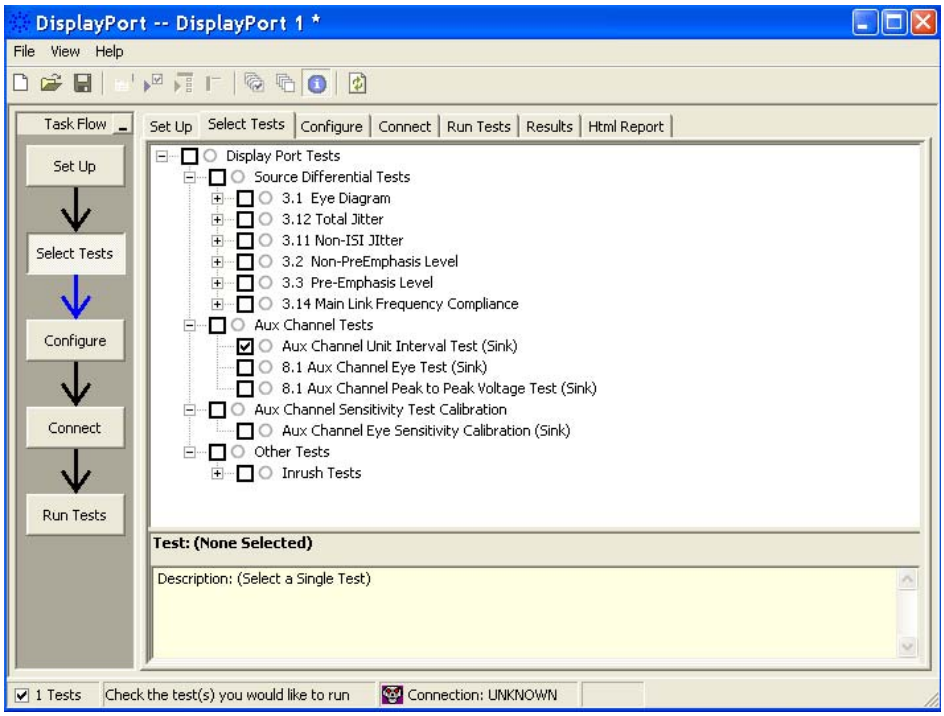
   c Connect probe from W2641B to an oscilloscope channel.

If reference source is not connected:

a Connect port **AUXp** & **AUXn** of fixture to the "**To Sink**" port labeled in the "**Sink Eye**" section of fixture W2641B.

b Connect port **p & n** in the "**Sink Eye to Scope**" section in fixture W2641B.

4 Go to "Select Tests" tab of compliance application. Navigate to "Aux Channel Unit Interval Test (Sink)".



5 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

400 ns < AUX Unit Interval < 600 ns.

Sink Aux Channel Eye Test (Normative)

This section provides the guidelines for sink Aux channel eye test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate the Aux channel to ensure that the timing and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.

Test Procedure

1 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up for Aux Channel tests procedures and parameters as shown in "Setting Up for Aux Channel Tests" on page 224.

3 If reference source is connected:

   a Connect **Ap**(Source AUX+) & **An**(Source AUX-) to Port **p & n** of the "**AUX Sensitivity Source**" section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the "**AUX Sensitivity Sink**" section of the W2641B fixture.

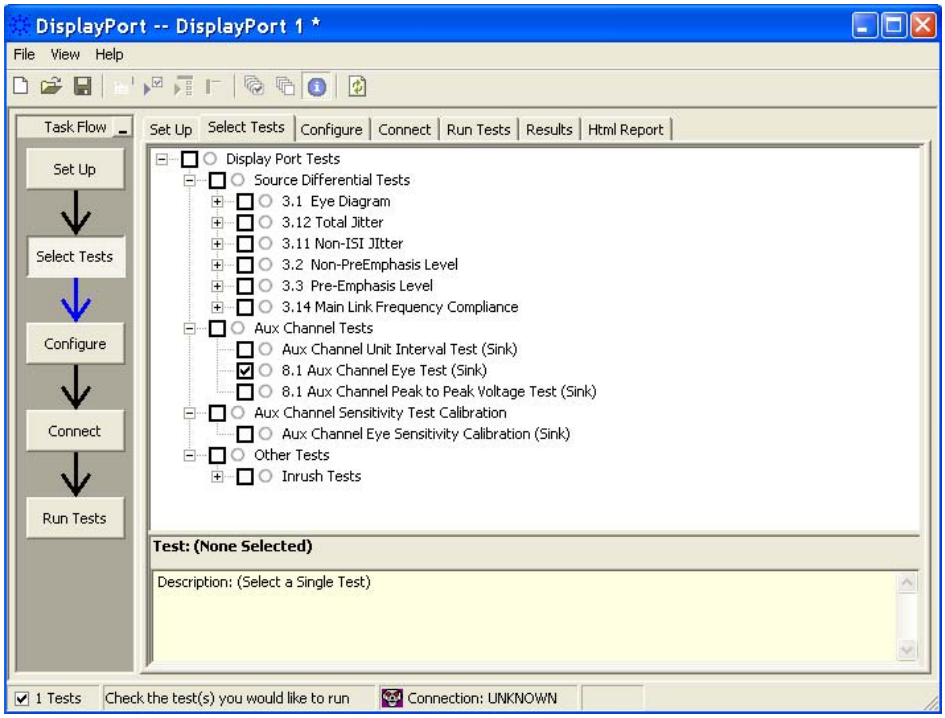
   c Connect probe from W2641B to a channel of oscilloscope.

   If reference source is not connected:

   a Connect port **AUXp** & **AUXn** of fixture to the "**To Sink**" port labeled in the "**Sink Eye**" section of fixture W2641B.

   b Connect port **p & n** in the "**Sink Eye to Scope**" section in fixture W2641B.

4 Go to “Select Tests” tab of compliance application. Navigate to “8.1 Aux Channel Eye Test (Sink)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

Mask Point	Coordinates
1	0.13, 0
2	0.23, 0.135
3	0.77, 0.135
4	0.87, 0
5	0.77, -0.135
6	0.23, -0.135

Mask Test: Zero mask failures.

Sink Aux Channel Peak-to-Peak Voltage Test (Normative)

This section provides the guidelines for sink Aux channel peak-to-peak voltage test using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To evaluate the Aux channel peak-to-peak voltage of a DisplayPort system.

Test Procedure

1 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux channel test procedures and parameters as shown in "Setting Up for Aux Channel Tests" on page 224.

3 If reference source is connected:

   a Connect **Ap**(Source AUX+) & **An**(Source AUX-) to Port **p & n** of the "**AUX Sensitivity Source**" section of the W2641B fixture with an SMP to SMP cable.

   b Connect port **AUXp** & **AUXn** to port **p & n** of the "**AUX Sensitivity Sink**" section of the W2641B fixture.

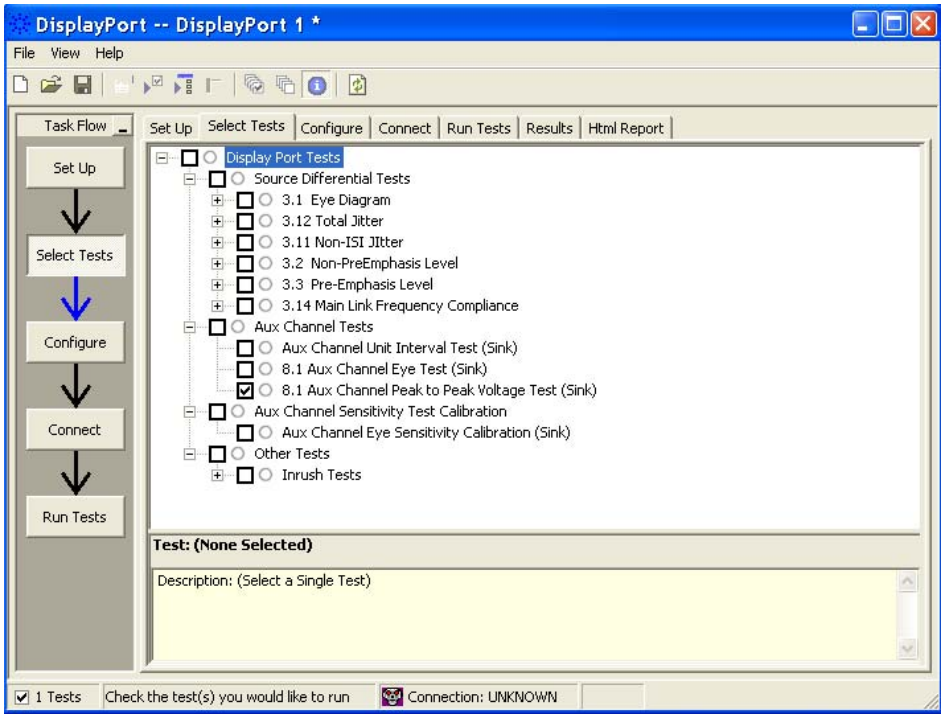
   c Connect probe from W2641B to an oscilloscope channel.

   If reference source is not connected:

   a Connect port **AUXp** & **AUXn** of fixture to the "**To Sink**" port labeled in the "**Sink Eye**" section of fixture W2641B.

   b Connect port **p & n** in the "**Sink Eye to Scope**" section in fixture W2641B.

4 Go to “Select Tests” tab of compliance application. Navigate to “8.1 Aux Channel Peak-to-Peak Voltage Test (Sink)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Pass Condition

Vpp(Sink) ≥ 290 mV.

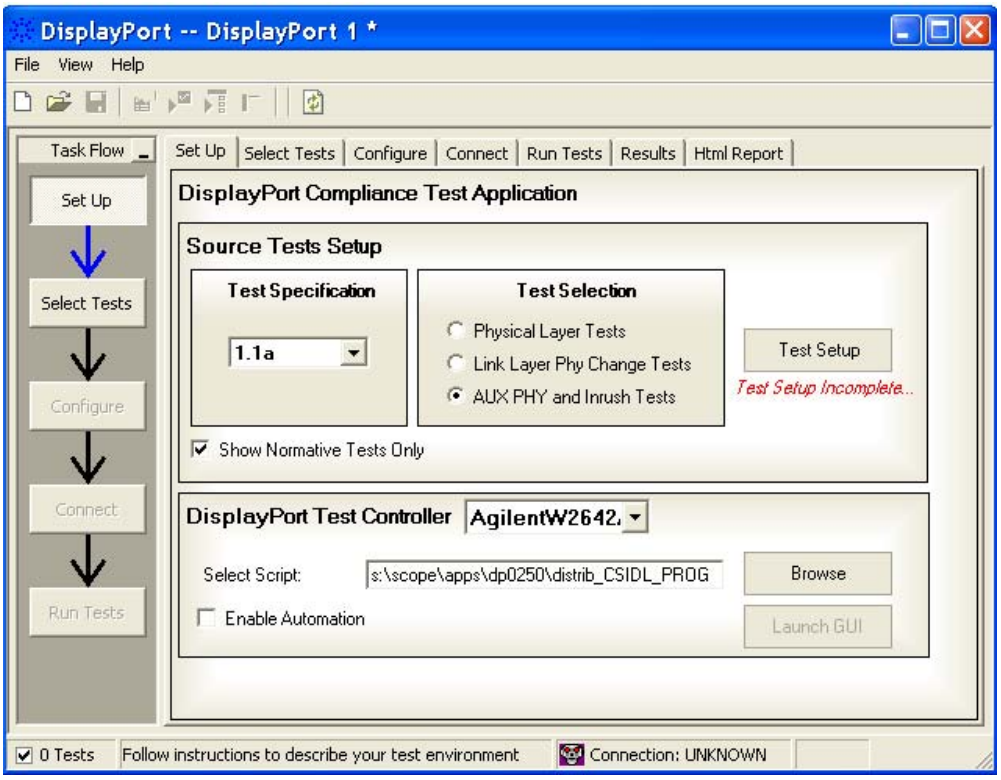
27
Aux Channel Sensitivity Tests

Setting Up for Aux Channel Sensitivity Tests

Before performing the Aux Channel Sensitivity tests, you must go through the set up process.

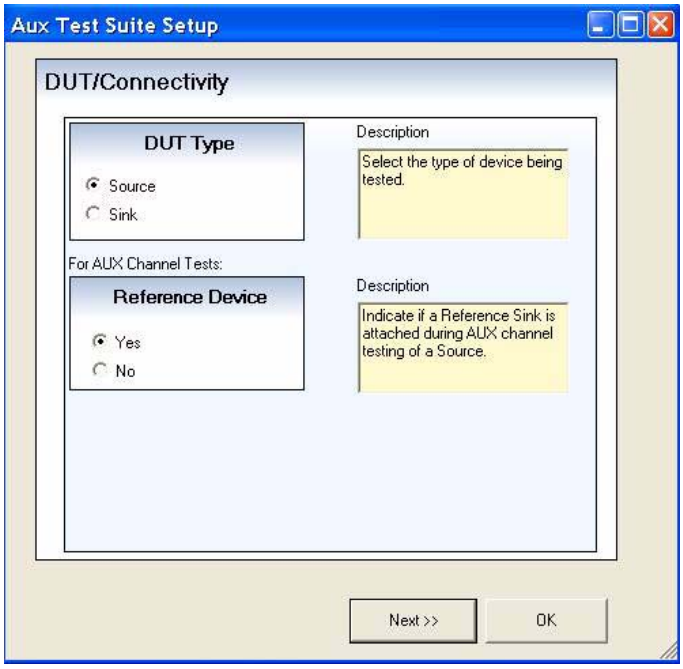
To set up for the Aux Channel Sensitivity tests:

1 Go to “Set Up” tab. Select **AUX PHY and Inrush Tests** in the Test Selection area; then, click the corresponding **Test Setup** button.



2 In the DUT/Connectivity setup page,

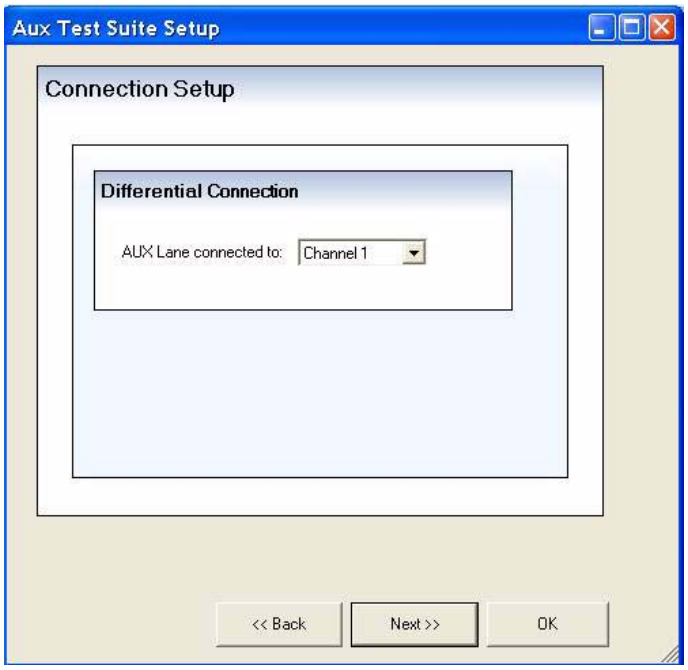
a define the device being tested (either a **Source** or a **Sink**).



b In the Reference Device area, select **Yes**. This is a requirement for Aux Channel Sensitivity tests.

c Click **Next** to go to next page.

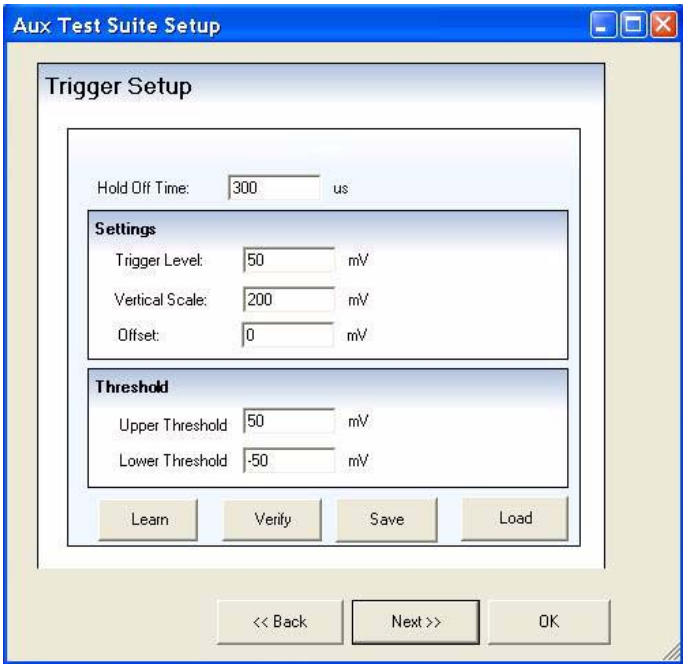
3 Next, in the Connection Setup page, select the oscilloscope channel that is used for the tests.



NOTE Ensure that all connections have been made before proceeding.

4 In the Trigger Setup page:

a you can click on the **Learn** button and follow the on-screen instructions, unless you know the trigger settings are correct.



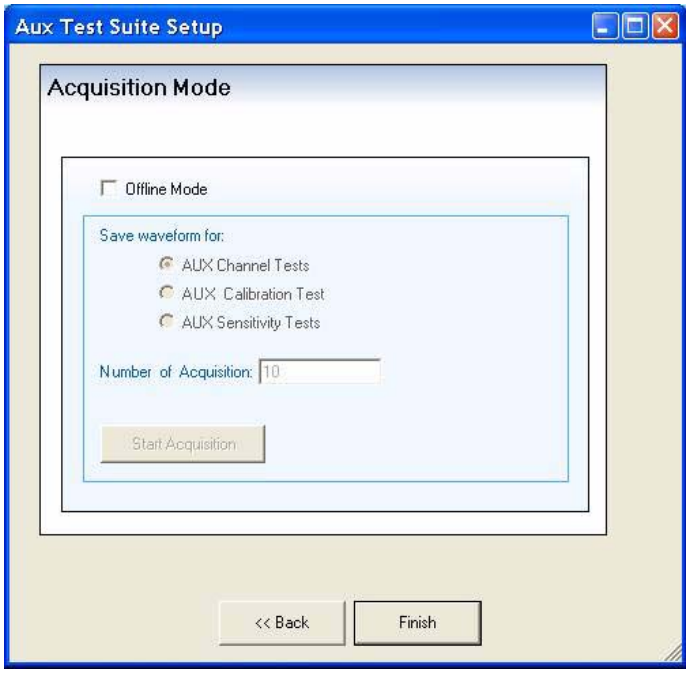
b When you are asked to initiate an Aux transaction, follow the procedure in "Initiating Aux Channel Transactions" on page 269. These steps determine the correct levels for Trigger, Vertical, and Thresholds.

c When you are certain the settings are correct, you can click **Verify** to check them.

d You can **Save** or **Load** the trigger setup configuration as a *.tsf file.

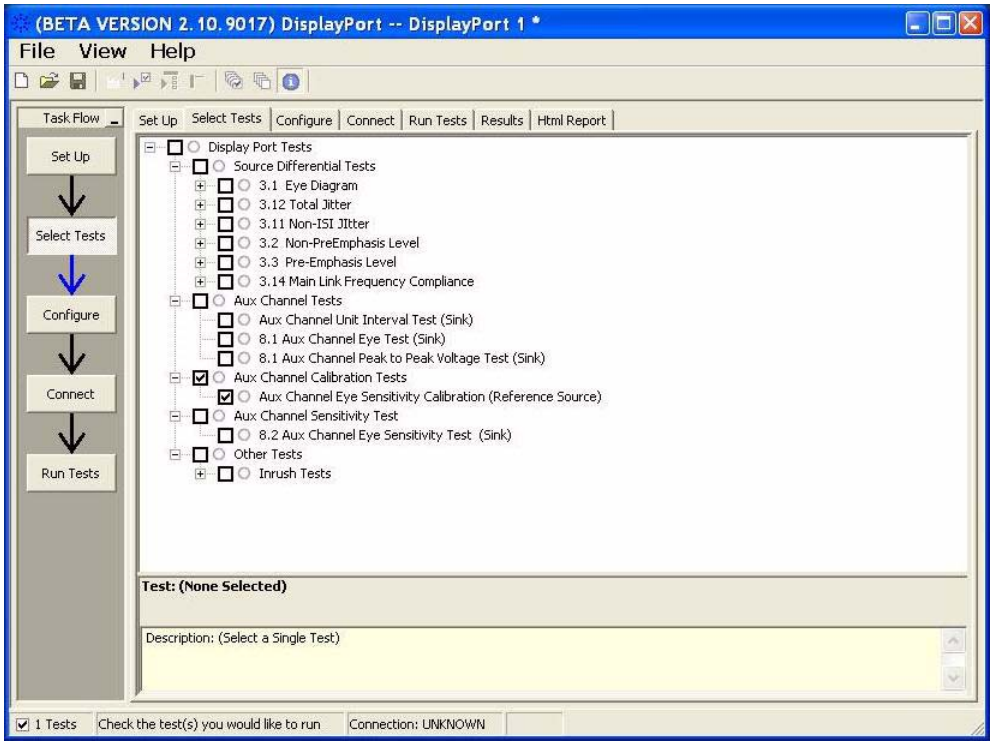
5 Lastly, in the Acquisition Mode page, enable Offline Mode if you prefer to collect the data first and process it later.

Once you have finished collecting data, if the Offline Mode is enabled, the tests will process the stored waveforms.

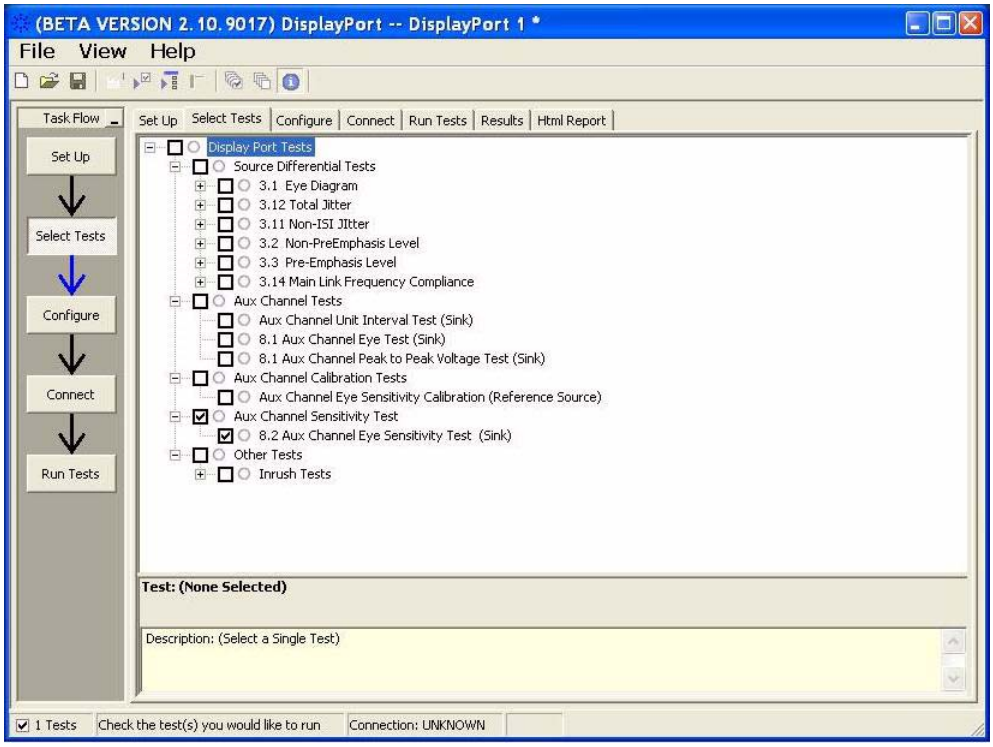


Click **Finish** when done.

6 Go to “Select Tests” tab. Navigate to “Aux Channel Calibration Tests”. This will also select “Aux Channel Eye Sensitivity Calibration”. The type, “(Reference Source)” or “(Reference Sink)”, depends on the DUT type specified earlier.



Then, navigate to “Aux Channel Sensitivity Test”. This will also select “8.2 Aux Channel Eye Sensitivity Test”. The type, “(Sink)” or “(Source)”, depends on the DUT type specified earlier.



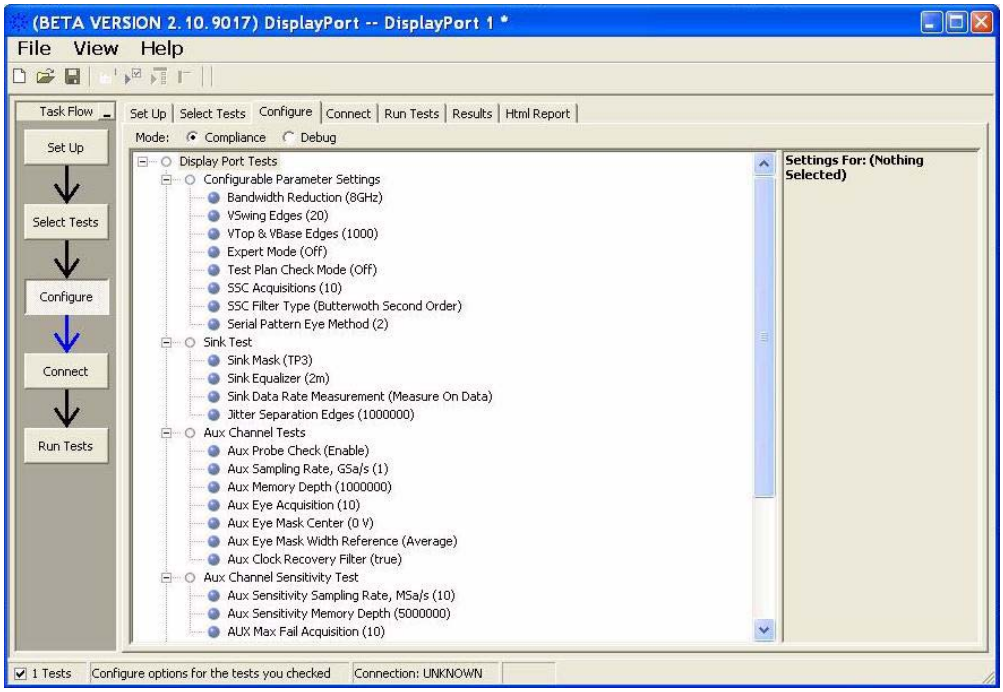
7 Go to “Configure” tab. Under “Aux Channel Sensitivity Tests”, these parameters can be modified:

Aux Sensitivity Sampling Rate, MSa/s (10) – change the sample rate, if desired.

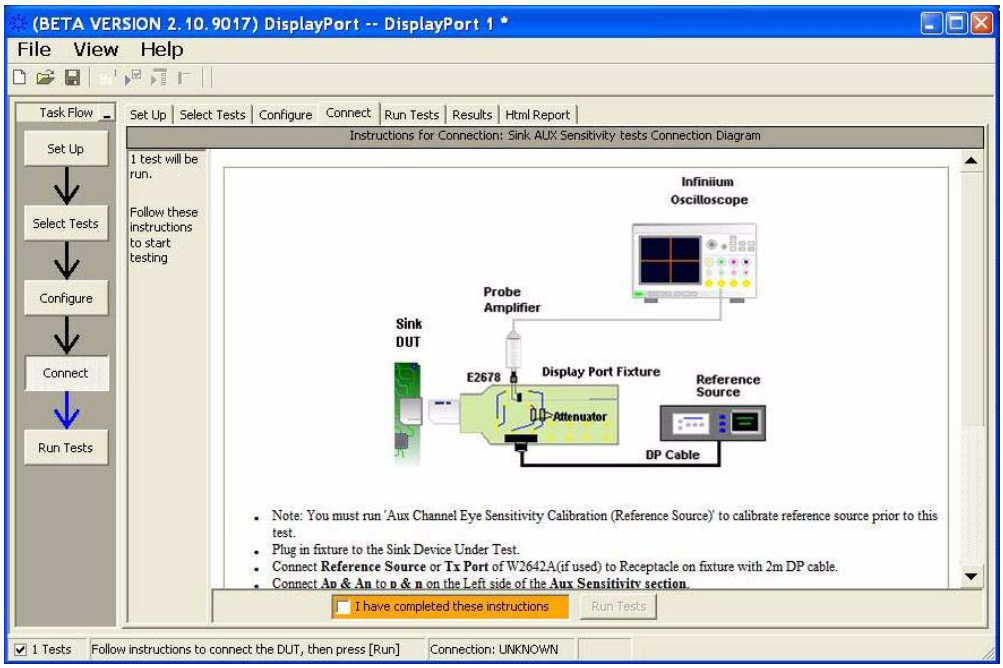
Aux Sensitivity Memory Depth (5000000) – select the different amount of capture memory to use for each acquisition, if desired.

AUX Traffic Decode Count (10) – change the number of traffics required before the test completes. The Compliance Test Specification requires 1000 for full compliance. If the test is done manually, you can consider reducing the number.

AUX Min Failure Required (10) – set the number of minimum number of failures required to abort the tests. When failure in an Aux sensitivity test is detected, you can stop the Aux traffic decoding immediately to save test time.



8 Go to “Connect” tab. Set up the connections as indicated in the connection diagram. Instructions will be displayed based on the test selected.



Select “I have completed these instructions” and click **Run Tests**.

Reference Sink Aux Channel Sensitivity Calibration

Probing/Connection Setup for Aux Channel Sensitivity Calibration

When performing the Aux Channel Sensitivity Calibration, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. The Source DUT must be connected so that the Reference Sink output level is calibrated against the loading of the device that will be tested.

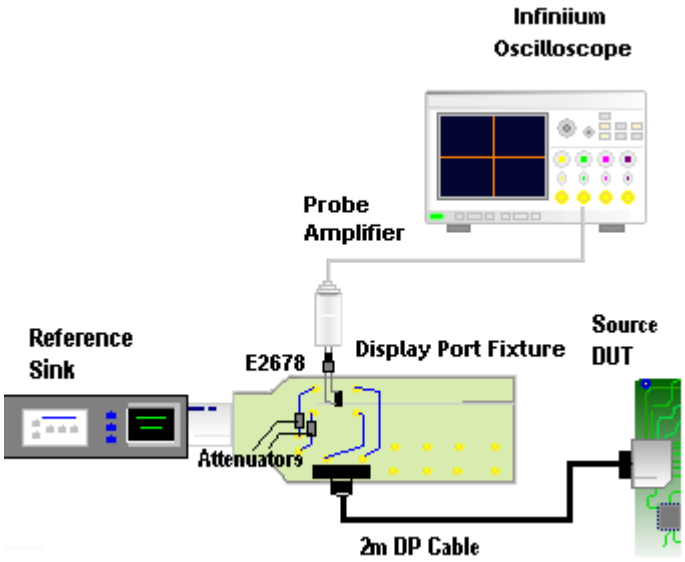


Figure 91 Connection diagram for calibrating reference sink connected to DUT source

Reference Sink Aux Channel Sensitivity Calibration

This section provides the guidelines to calibrate reference sink prior to performing Aux Channel Sensitivity tests for a Source DUT using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To adjust Reference Sink AUX channel V_{Swing} to 270 mV +10 mV/-30 mV prior to performing AUX Channel Sensitivity tests on a DUT Source. This test reports the difference between the current V_{Swing} and the required level of 270 mV. This test will help you adjust the voltage to reach the required level.

Test Procedure

1 Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in “Setting Up for Aux Channel Sensitivity Tests" on page 248.

3 Ensure that the DUT Source is connected so that the **“Reference Sink”** output level is calibrated against the loading of the device to be tested.

4 Connect the DUT Source as follows:

   a Connect “**Fixture Plug**” to “**Reference Sink**” or **DisplayPort Rx** port on W2642A (if used).

   b Connect “**Fixture Receptable**” to “**DUT Source**” with a 2 m DP cable.

   c Connect port **AUXp** & **AUXn** to port **p & n** on the left side of the “**AUX Sensitivity**” section, using cables and attenuators as follows:

      i Connect a pair of SMA-SPA cables to two attenuators. Start with 7 dB.

      ii Connect two SMP ends to port **AUXp** & **AUXn**, and the other ends to port **p & n**.

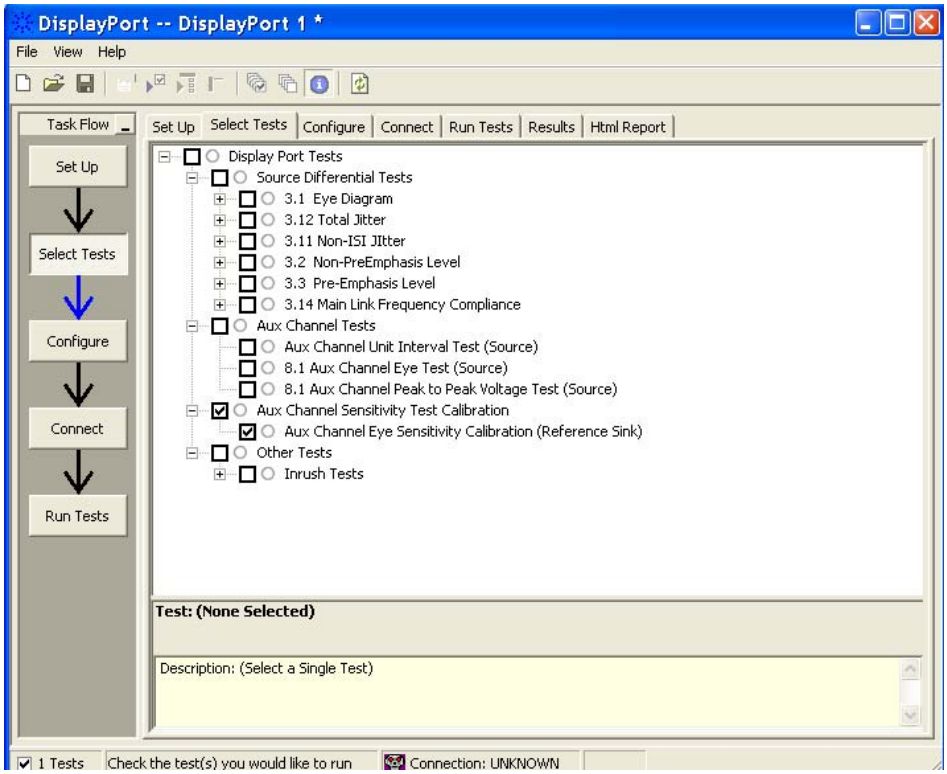
      iii Insure polarity is correct.

   d Connect port **p & n** on the right side of the “**AUX Sensitivity**” section to port **Ap & An**, using two short SMP cables and insure polarity is correct.

   e Connect **E2678A Socketed Probe** to the left side of the 2-pin header in the **“Aux Sensitivity”** section. These are the two pins closest to the DP Plug.

   f Connect **E2678A Socketed Probe** to **Differential 1168/1169 Amplifier** and then to a channel on the scope.

5 Go to “Select Tests” tab of compliance application. Navigate to “Aux Channel Eye Sensitivity Calibration (Reference Sink)”.



6 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

7 You will receive an error at the end of the test, if the measured V_{Swing} is above 280 mV or below 240 mV.

8 The error message tells you how much voltage is needed to increase or decrease to be close to the required level of 270 mV for the AUX Sensitivity test. In the range of around 270 mV, a 1 dB attenuator produces a change of about 30 mV.

9 You can apply attenuators or other means to decrease or increase voltage.

10 Once voltage is adjusted, you are required to re-run the same test until it passes.

Pass Condition

$240\ mV \leq V_{Swing} \leq 280\ mV$.

Reference Source Aux Channel Sensitivity Calibration

Probing/Connection Setup for Aux Channel Sensitivity Calibration

When performing the Aux Channel Sensitivity Calibration, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. The Sink DUT must be connected so that the Reference Source output level is calibrated against the loading of the device that will be tested.

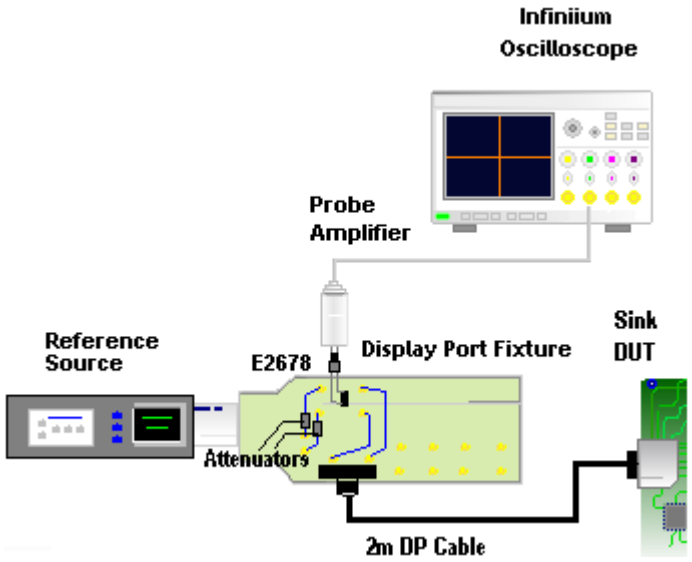


Figure 92 Connection diagram for calibrating reference source connected to DUT sink

Reference Source Aux Channel Sensitivity Calibration

This section provides the guidelines to calibrate reference source prior to performing Aux Channel Sensitivity tests for a Sink DUT using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To adjust Reference Source AUX channel V_{Swing} to 270 mV +10 mV/-30 mV prior to perform AUX Channel Sensitivity tests on a DUT Sink. This test reports the difference between the current V_{Swing} and the required level of 270 mV. This test will help you adjust the voltage to reach the required level.

Test Procedure

1 Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in “Setting Up for Aux Channel Sensitivity Tests" on page 248.

3 Ensure that the DUT Sink is connected so that the **“Reference Source”** output level is calibrated against the loading of the device to be tested.

4 Connect the DUT Sink as follows:

   a Connect “**Fixture Plug**” to “**Reference Source**” or **DisplayPort Tx** port on W2642A (if used).

   b Connect “**Fixture Receptable**” to “**DUT Sink**” with a 2 m DP cable.

   c Connect port **AUXp** & **AUXn** to port **p & n** on the left side of the “**AUX Sensitivity**” section, using cables and attenuators as follows:

      i Connect a pair of SMA-SPA cables to two attenuators. Start with 7 dB.

      ii Connect two SMP ends to port **AUXp** & **AUXn**, and the other ends to port **p & n**.

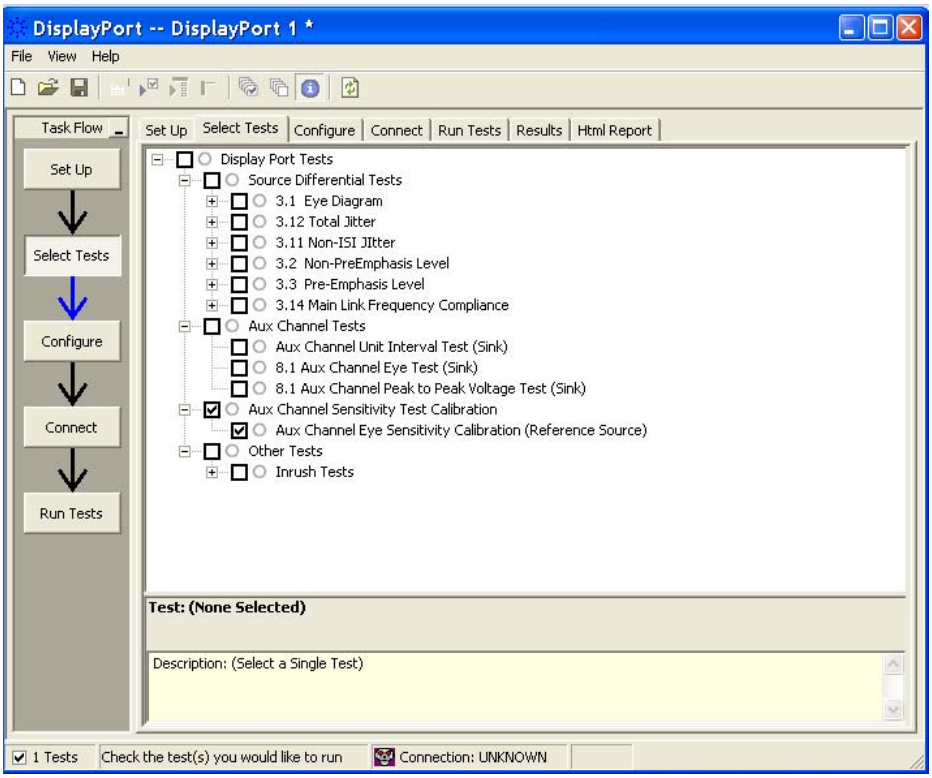
      iii Insure polarity is correct.

   d Connect port **p & n** on the right side of the “**AUX Sensitivity**” section to port **Ap & An**, using two short SMP cables and insure polarity is correct.

   e Connect **E2678A Socketed Probe** to the left side of the 2-pin header in the **“Aux Sensitivity”** section. These are the two pins closest to the DP Plug.

   f Connect **E2678A Socketed Probe** to **Differential 1168/1169 Amplifier** and then to a channel on the scope.

5 Go to “Select Tests” tab of compliance application. Navigate to “Aux Channel Eye Sensitivity Calibration (Reference Source)”.



6 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

7 You will receive an error at the end of the test, if the measured V_{Swing} is above 280 mV or below 240 mV.

8 The error message tells you how much voltage is needed to increase or decrease to be close to the required level of 270 mV for the AUX Sensitivity test. In the range of around 270 mV, a 1 dB attenuator produces a change of about 30 mV.

9 You can apply attenuators or other means to decrease or increase voltage.

10 Once voltage is adjusted, you are required to re-run the same test until it passes.

Pass Condition

240 mV $\leq V_{Swing} \leq$ 280 mV.

8.2 Aux Channel Eye Sensitivity Test (Source)

Probing/Connection Setup for Aux Channel Eye Sensitivity Test

When performing the Source Aux Channel Sensitivity test, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. Before running this test, insure that the Reference Sink AUX Channel Sensitivity Calibration has been performed.

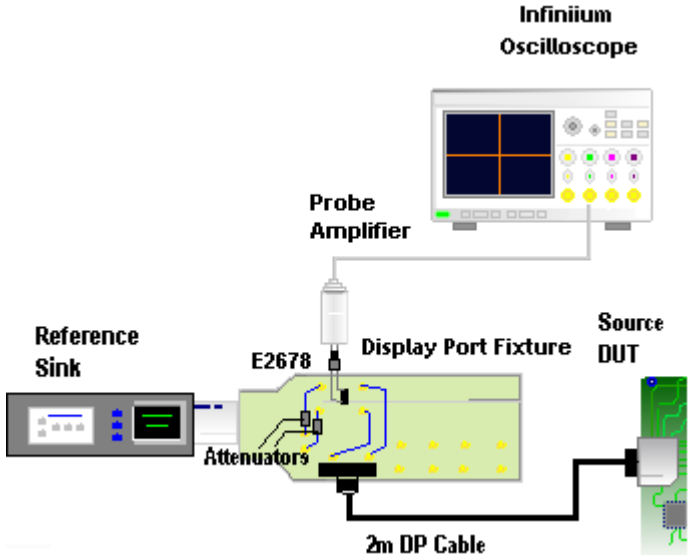


Figure 93 Connection diagram for Source AUX Channel Eye Sensitivity test

Source Aux Channel Eye Sensitivity Test (Normative)

This section provides the guidelines for Source Aux Channel Eye Sensitivity testing using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To determine that the AUX Channel of the Source DUT meets the Sensitivity requirement to reliably receive data at the 270 mV level required in Compliance Test Specification 1.2.

Test Procedure

1 Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in “Setting Up for Aux Channel Sensitivity Tests" on page 248.

3 Connect the DUT Source as follows:

   a Connect “**Fixture Plug**” to “**Reference Sink**” or **DisplayPort Rx** port on W2642A (if used).

   b Connect “**Fixture Receptable**” to “**DUT Source**” with a 2 m DP cable.

   c Connect port **AUXp** & **AUXn** to port **p & n** on the left side of the “**AUX Sensitivity**” section, using cables and attenuators as follows:

      i Connect a pair of SMA-SPA cables to two attenuators. Start with 7 dB.

      ii Connect two SMP ends to port **AUXp** & **AUXn**, and the other ends to port **p & n**.

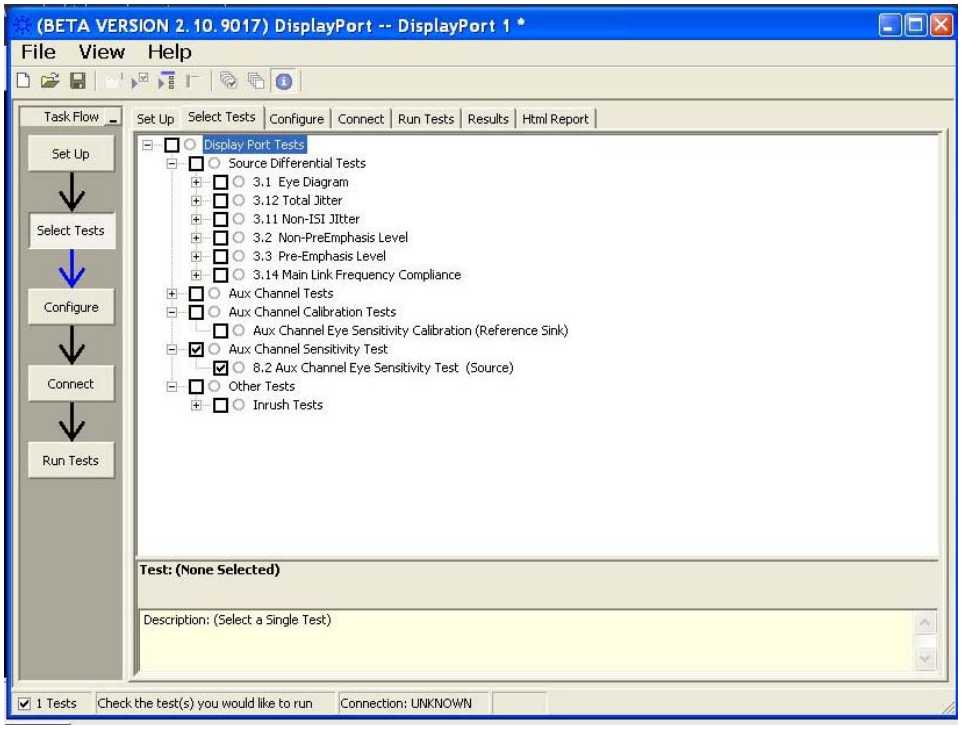
      iii Insure polarity is correct.

   d Connect port **p & n** on the right side of the “**AUX Sensitivity**” section to port **Ap & An**, using two short SMP cables and insure polarity is correct.

   e Connect **E2678A Socketed Probe** to the left side of the two-pin header in the **“Aux Sensitivity”** section. These are the two pins closest to the DP Plug.

   f Connect **E2678A Socketed Probe** to **Differential 1168/1169 Amplifier** and then to a channel on the scope.

4 Go to “Select Tests” tab of compliance application. Navigate to “Aux Channel Eye Sensitivity Test (Source)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

6 The software will verify that the Source is receiving requests from the Reference Sink correctly. Each time you are asked to initiate Aux transactions, use one of the techniques described under “Procedure for Initiating Aux Channel Transactions" on page 269.

7 For each request that repeats itself less than two times and then followed by a different request will be counted as a PASS. Any request that repeats itself for three times will be counted as a FAIL.

Pass Condition

1000 Aux transactions without errors.

8.2 Aux Channel Eye Sensitivity Test (Sink)

Probing/Connection Setup for Aux Channel Eye Sensitivity Test

When performing the Sink Aux Channel Sensitivity test, the DisplayPort Electrical Performance Compliance Test Application prompts you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. Before running this test, insure that the Reference Source Aux Channel Sensitivity Calibration has been performed.

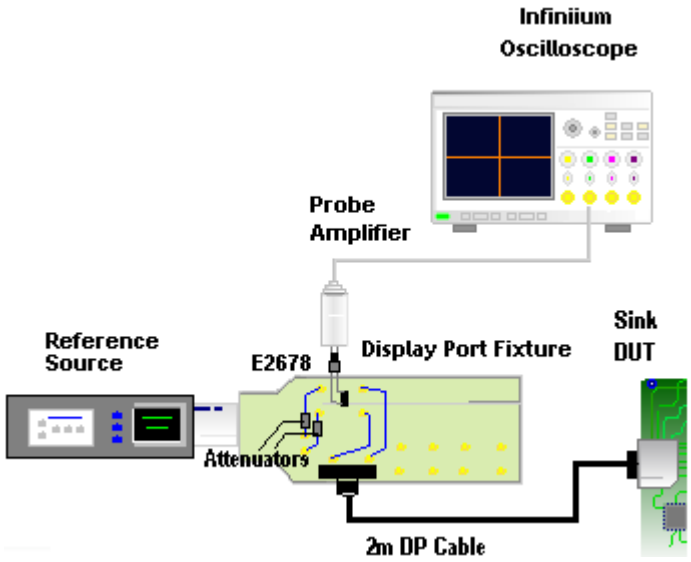


Figure 94 Connection diagram for Sink Aux Channel Eye Sensitivity test

Sink Aux Channel Eye Sensitivity Test (Normative)

This section provides the guidelines for Sink Aux Channel Eye Sensitivity testing using an Infiniium oscilloscope and the DisplayPort Electrical Performance Compliance Test Application.

Purpose

To determine that the Aux Channel of the Sink DUT meets the Sensitivity requirement to reliably receive data at the 270 mV level required in Compliance Test Specification 1.2.

Test Procedure

1 Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 24.

2 Set up Aux test procedures and parameters as shown in “Setting Up for Aux Channel Sensitivity Tests" on page 248.

3 Connect the DUT Sink as follows:

   a Connect “**Fixture Plug**” to “**Reference Source**” or **DisplayPort Rx** port on W2642A (if used).

   b Connect “**Fixture Receptable**” to “**DUT Sink**” with a 2 m DP cable.

   c Connect port **AUXp** & **AUXn** to port **p & n** on the left side of the “**AUX Sensitivity**” section, using cables and attenuators as follows:

      i Connect a pair of SMA-SPA cables to two attenuators. Start with 7 dB.

      ii Connect two SMP ends to port **AUXp** & **AUXn**, and the other ends to port **p & n**.

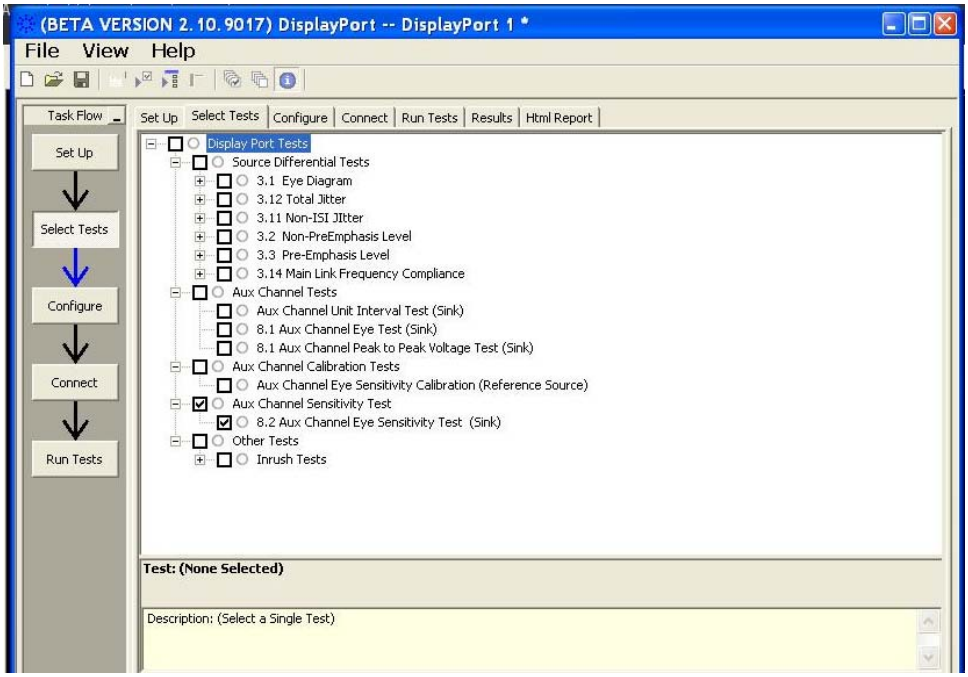
      iii Insure polarity is correct.

   d Connect port **p & n** on the right side of the “**AUX Sensitivity**” section to port **Ap & An**, using two short SMP cables and insure polarity is correct.

   e Connect **E2678A Socketed Probe** to the left side of the 2-pin header in the **“Aux Sensitivity”** section. These are the two pins closest to the DP Plug.

   f Connect **E2678A Socketed Probe** to **Differential 1168/1169 Amplifier** and then to a channel on the scope.

4 Go to “Select Tests” tab of compliance application. Navigate to “Aux Channel Eye Sensitivity Test (Sink)”.



5 Follow the DisplayPort Electrical Performance Compliance Test Application’s task flow to set up configuration options, make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

6 The software will verify that the Sink is receiving requests from the Reference Source correctly. Each time you are asked to initiate Aux transactions, use one of the techniques described under “Procedure for Initiating Aux Channel Transactions" on page 269.

7 For each request that has a valid reply, the software will count it as a PASS. Any request not followed by a reply will be counted as a FAIL. You may stop the loop anytime by clicking **Cancel** or **Stop**.

Pass Condition

1000 Aux transactions without errors.

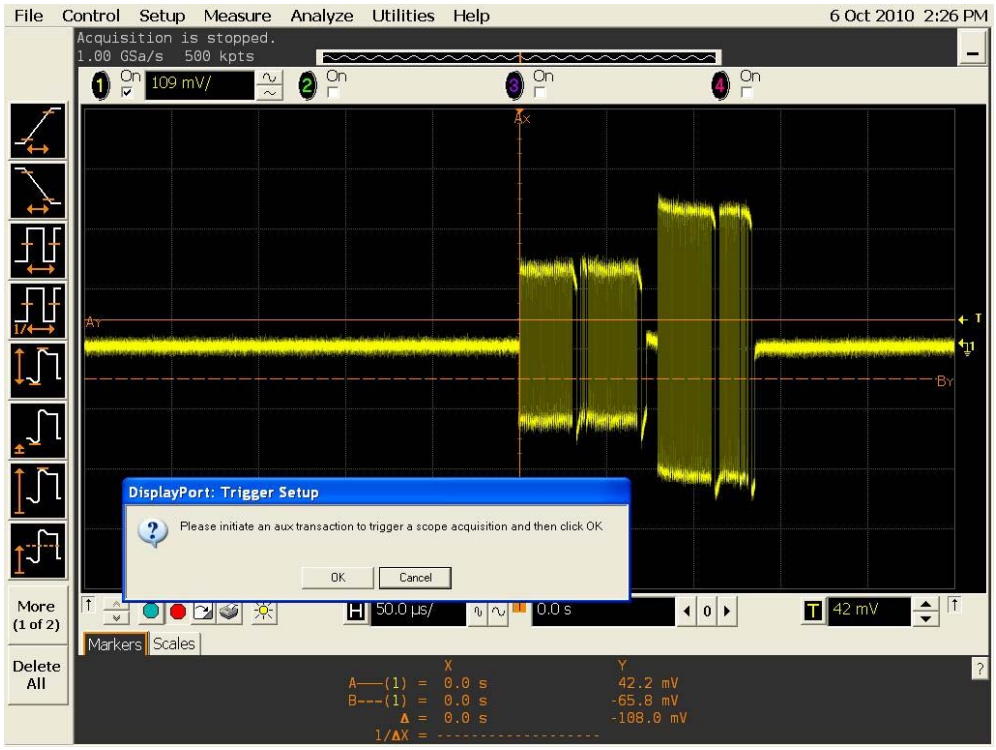
Initiating Aux Channel Transactions

Procedure for Initiating Aux Channel Transactions

When the software prompts, “Please initiate an Aux transaction to trigger an acquisition”, use one of the following techniques and then click **OK**.

1 For a Source DUT, if the W2642A/QD882E is available, use the DisplayPort Test Controller to send a HPD pulse.

2 For a Sink DUT, if the W2642A/QD882E is available, use the DisplayPort Test Controller to send a read request.



3 If you are using any other DP device as a Reference Sink or Source, unplug the Reference device from the DUT and plug it in again.

4 If no Aux traffic is displayed on the scope screen:

a Return to "Set Up" tab.

b Click the corresponding **Setup** button in the “Aux and Other Tests Setup” area.

c Advance to the “Trigger Setup” page.

d Click on the **Learn** button and follow the on-screen instructions to determine the correct trigger settings for these tests.

28
DP Inrush Tests

DP Inrush Tests

Probing/Connection Setup for DP Inrush Tests

When performing the DP Inrush test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

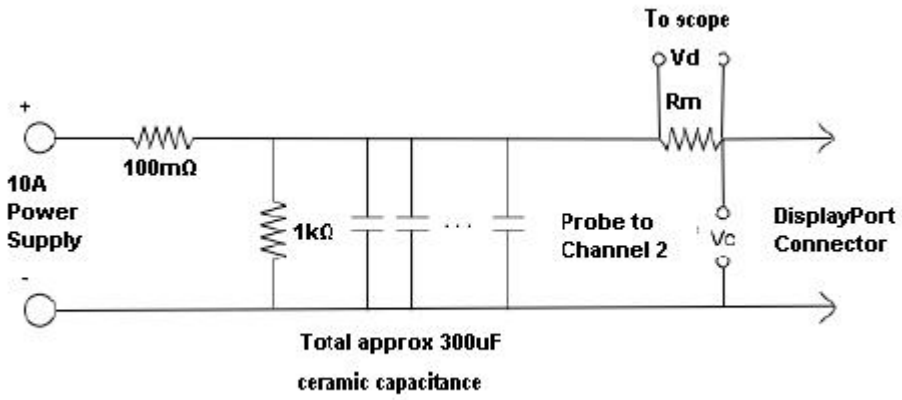


Figure 95 Connection diagram when performing DP Inrush tests

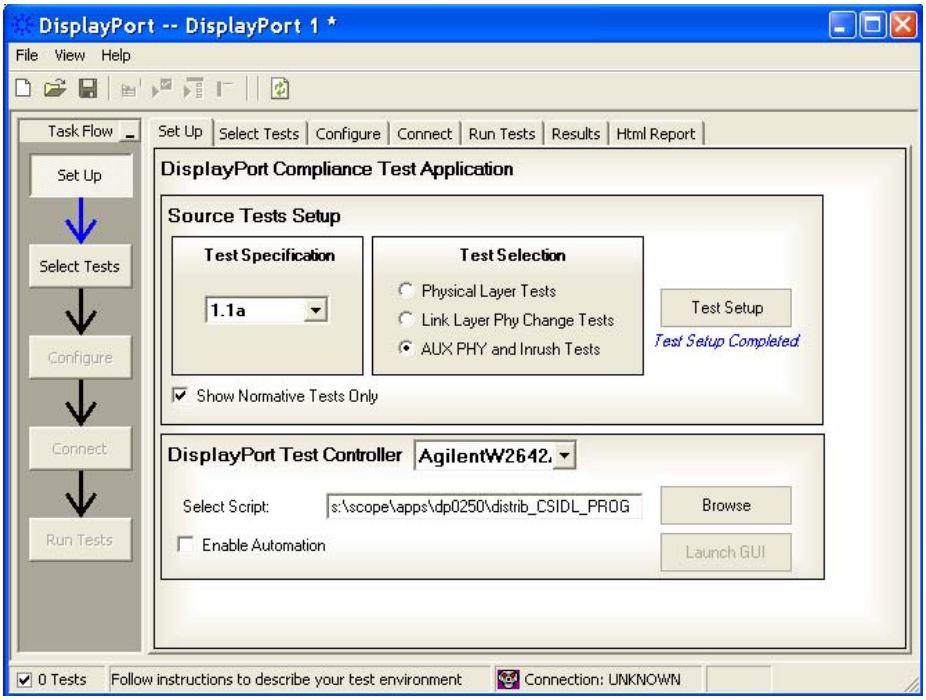
Inrush Current Tests (Informative)

Purpose

To evaluate the Inrush Energy at the power supply input of a power-consuming device under test, or the inrush tolerance at the power supply output of a power-providing device under test. For power-consuming devices, such as dongles, Inrush Power Energy and Peak Inrush Current will be measured. Power providers, such as laptops, must continue to operate through a plug-in event.

Test Procedure

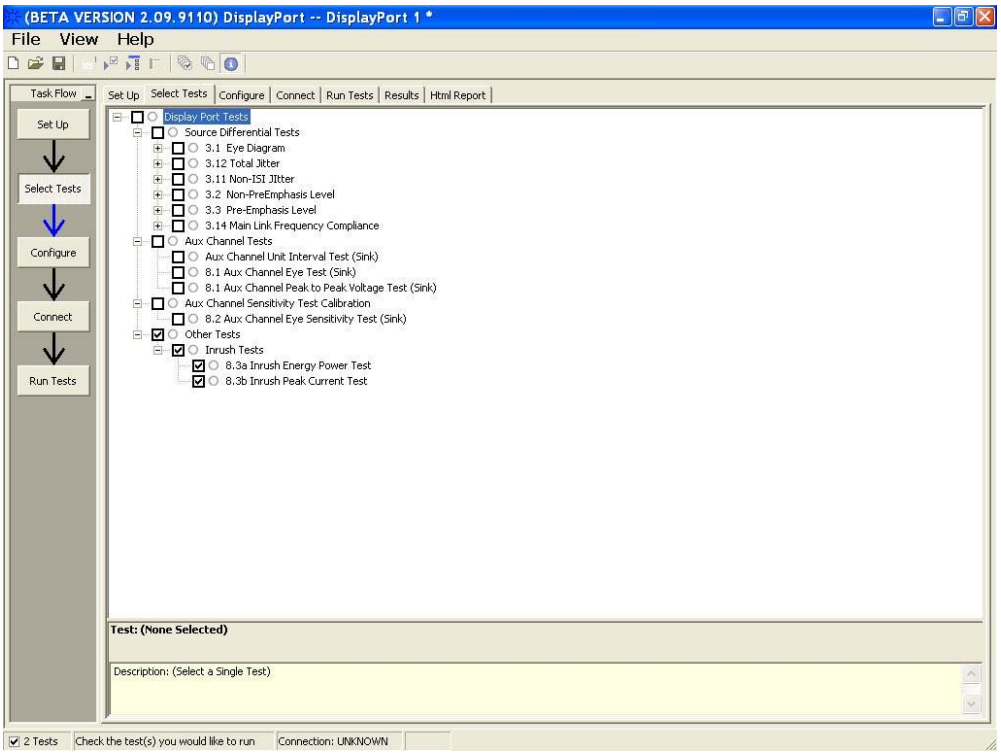
1 On the DisplayPort Compliance application main page, select **AUX PHY and Inrush Tests** in the Test Selection area; then, click the corresponding **Test Setup** button.



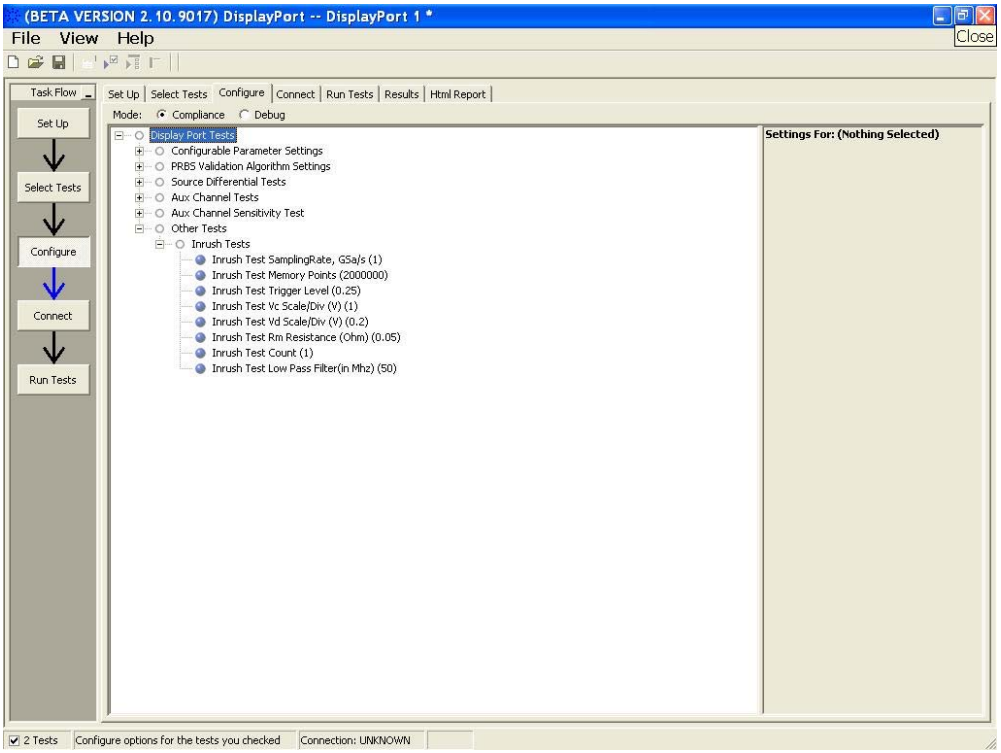
2 Go to “Select Tests” tab of compliance application. Navigate to “Inrush Tests”. This will select the following two tests:

a 8.3a Inrush Energy Power Test

b 8.3b Inrush Peak Current Test



3 Change the setting in “Configure” tab.



a Click on “Other Tests” to expand the menu.

b Click on “Inrush Tests” to expand the choices.

c Normally, you do not need to change the first two selections:

i Inrush Test Sampling Rate, Gsa/s (1) – change the scope sampling rate.

ii Inrush Test Memory Points (2000000) – change the length of acquisition by memory points.

d Once you determine the optimum levels for the DUT, you can change the next three selections:

i Inrush Test Trigger Level (0.25)

ii Inrush Test V_c Scale/Div (V) (1) – voltage applied to the device.

iii Inrush Test V_d Scale/Div (V) (0.2) – voltage proportional to current draw.

e The default setting for R_m as shown in Figure 95 is 50 mΩ. In cases where V_d is not measured across a 50 mΩ resistor, for example, when using the N2782A 0.1 A/V current probe, you need to set R_m to 1.0 by changing the following selection:

   i Inrush Test R_m Resistance (Ω) (0.05)

f The following selection can be changed if you want to shorten the test when debugging. Set the value to 10 for compliance testing.

   i Inrush Test Count (10)

g Change the following selection for debugging purpose. Set the value to 50 MHz for the E2678A high bandwidth probe.

   i Inrush Test Low Pass Filter in MHz (50)

4 Go to "Connect" tab. Set up the connections as indicated in the connection diagram.

If you are using V-Prime test fixture, connect as follows:

a Ch1: Measure V_d using the E2678A and 1168/1169 to probe P1, I_SNS_+, and I_SNS_-. (E2678A Pos + to I_SNS_+ for Sink. Reverse for Source.)

b Ch2: Measure V_c using a cut off coax cable on J1 connected to the E2678A and 1168/1169 (or probe center of J1 and GND with short wires).

c On the scope software, click **Scope > Setup > Channel1/2 > Probes**.

d Verify that the E2678A Df Sckt head is selected for both.

Alternately, you can set up this test using a current probe and V-Prime fixture:

a Ch1: Measure V_d using the N2782A current probe and E2697A high impedance adapter. (Clamp wire CL1 with the arrow facing LEDs for Sink. Reverse for Source.)

b Ch2: Measure V_c at P1, I-SNS+, and GND with the E2678A and 1168/1169.

c On the scope software, click **Scope > Setup > Channel1/2 > Probes**.

   i Verify Channel 1 = 0.1 V/A Current Probe + E2679A 1 mΩ Converter, Attn 1:1.

   ii Verify Channel 2 = E2678A Df Sckt head.

5 Once the connection is verified correctly, select "I have completed these connections" and click **Run Tests**.

6 When prompted with “Please initiate a hot plug”, unplug and then plug in the DUT to the test fixture, or on the V-Prime fixture, press the appropriate button.

   a S1 = Blue, for a Sink DUT

   b S2 = Gray, for a Source DUT

   Verify that the current and voltage traces are displayed and then click **OK**.

7 If no current or voltage traces are displayed:

Optimize Display Scaling:

   a You may need to expand the horizontal scale to see these traces (try 20 µs).

   b If one or both of the top two traces are still missing, verify the polarity of the Channel 1 probe is correct. It needs a positive edge to trigger.

   c Change the Trigger Sweep mode to “Triggered”. Try “Auto”, if “Triggered” does not produce anything, then go back to “Triggered”.

   d Repeat the hot plug or press the button.

   e Adjust Ch1 & Ch2 Scale, Trigger Level, and Horizontal Scale until the trace capture is repeatable and Ch1 & Ch2 fit the top half of their graph.

   f Note the settings that work.

   g Set the Trigger Sweep mode back to “Single” and then, click **OK**.

   h To set up the software to use different settings, complete the measurement, then go to the Configure tab. Under “Other Tests”, select “Inrush Tests”:

      i Change Trigger Level, V_c Scale, and V_d Scale to match the values noted above.

      ii The next time you run the Inrush tests, these new values will be used.

   j If you are told that the signal is being triggered but the scale is not optimized, in the Scope main menu select **Setup > Channel 1**:

      i Enter a scaling factor that makes Channel 1 nearly fills the top graph. For example, if the signal is 11 A, enter 3 V/div.

Verify Marker Positions for Integration:

a When you are asked to:

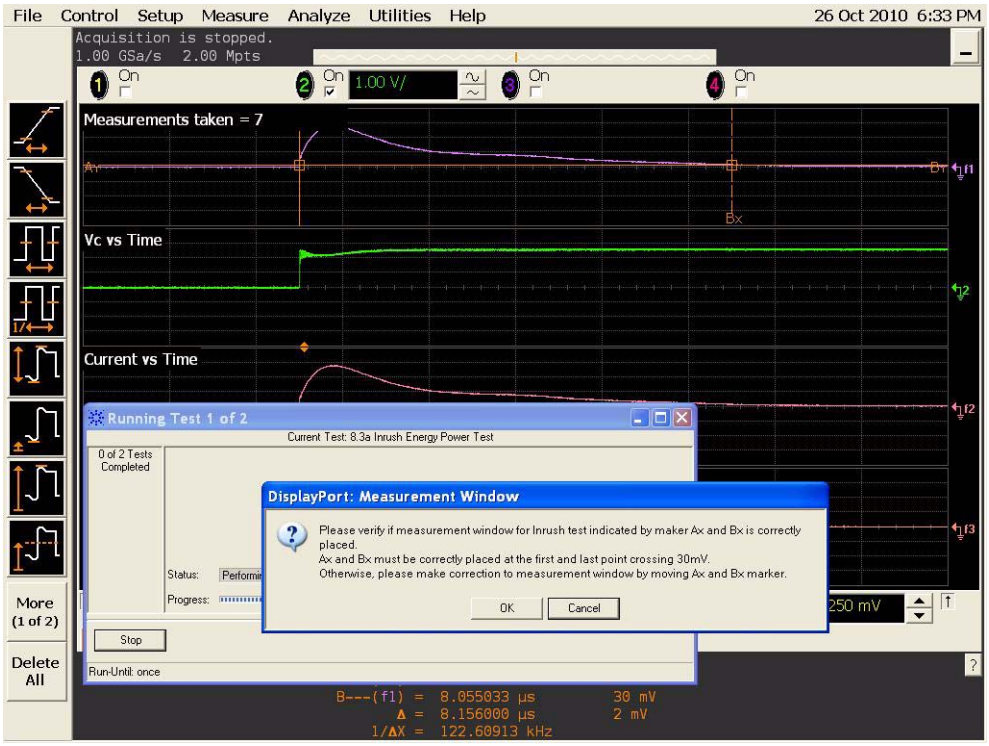
i "Verify measurement window ... indicated by markers Ax & Bx is correctly placed",

- Verify that the A and B markers are placed on the Ch1 trace that rises quickly and then decays.
- Marker Ax should be placed on the Ch1 trace that rises quickly from time 0 and at the point crossing marker Ay (30 mV if R_m is 50 mΩ).
- Marker Bx should be placed on the Ch1 trace that decays and at the point crossing marker Ay (30 mV if R_m is 50 mΩ).
- If not, drag the vertical bar associated with the Bx marker to the right until you find the first occurrence of a Y value that crosses marker Ay.

b Now these two markers bound the area under the current curve to be integrated.

c Click **OK**.

d The software will calculate energy and peak current, and record the results.



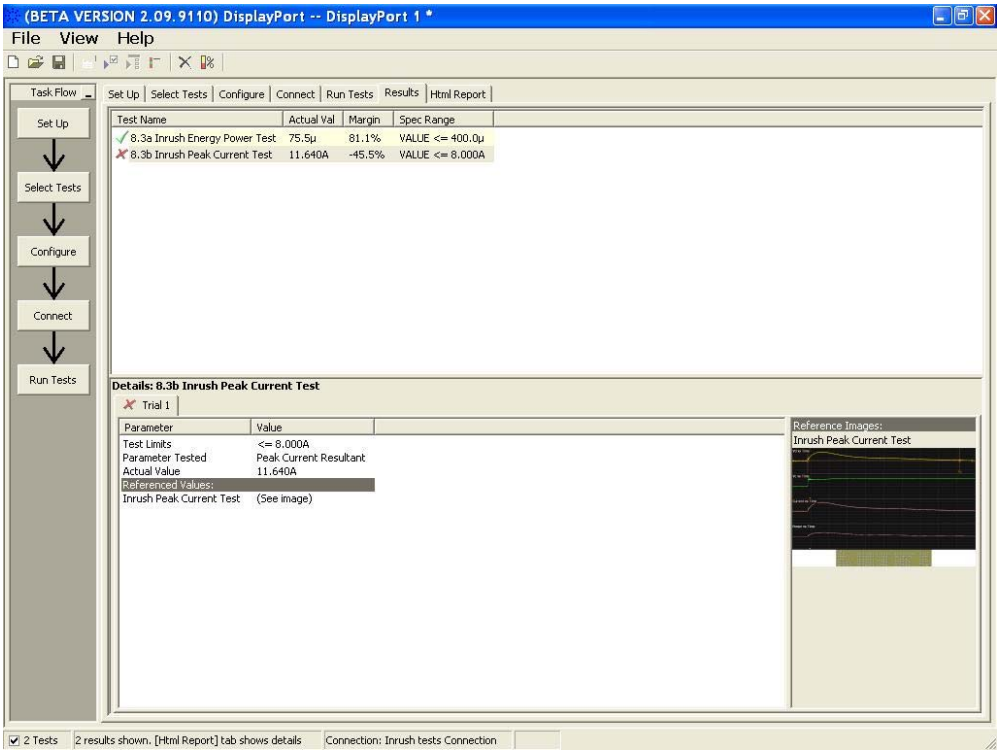
Results Tab and Html Report Tab:

a Click **OK** when "All selected tests completed" is displayed.

b View results:

i The Results tab summarizes the results for this test.

ii The Html Report tab brings up a report that includes the screen capture.



Pass Condition

During 10 reconnection events, the following conditions must be met.

Power-Consuming Device:

- Energy Power less than 400 µJ (Normative)
- Peak Current less than 8 A (Informative)

Power-Providing Device:

- Must exhibit normal operation during all plug-in events.

29 Calibrating the Infiniium Oscilloscope and Probe

This chapter describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DisplayPort automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Agilent Infiniium oscilloscopes).
- E2655A/B probe de-skew fixture.
- 82 Ω damping resistors (01130-81506) for the Socketed Differential Probe Head.

Figure 96 below shows a drawing of the above connector items.

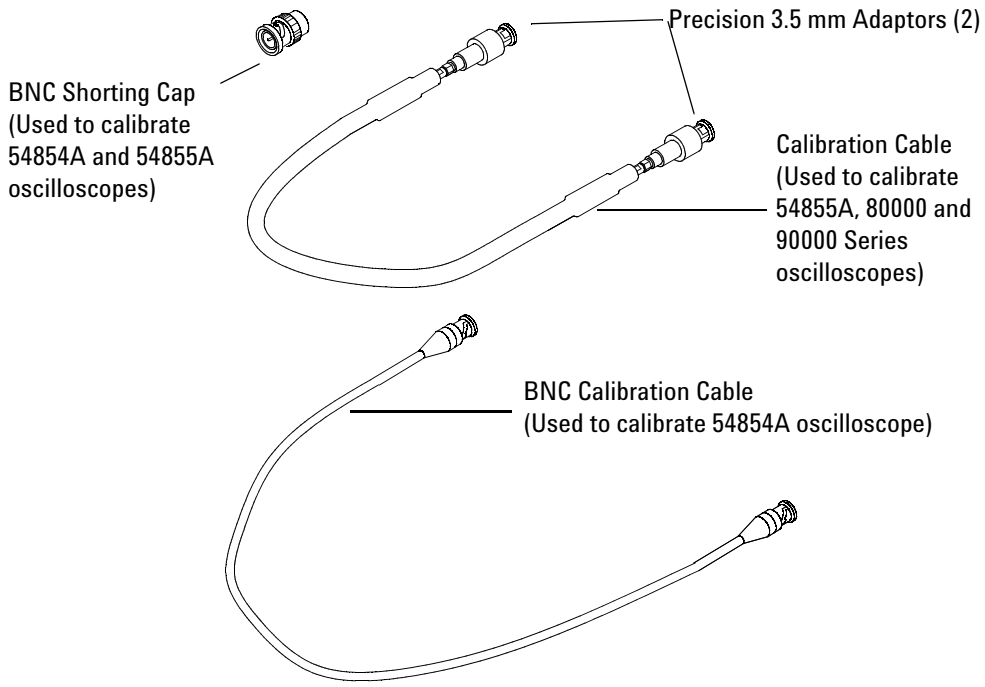


Figure 96 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b If a second monitor is being used, connect it to the VGA connector located near the LAN port, on the rear of the oscilloscope.

   c Plug in the power cord.

   d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 2 below.

2 Locate and prepare the accessories that will be required for the internal calibration

   a Locate the calibration cable.

   b Locate the two Agilent precision SMA/BNC adapters.

   c Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   d Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 97 below, perform the following steps:

a Click on the **Utilities>Calibration** menu to open the Calibration window.

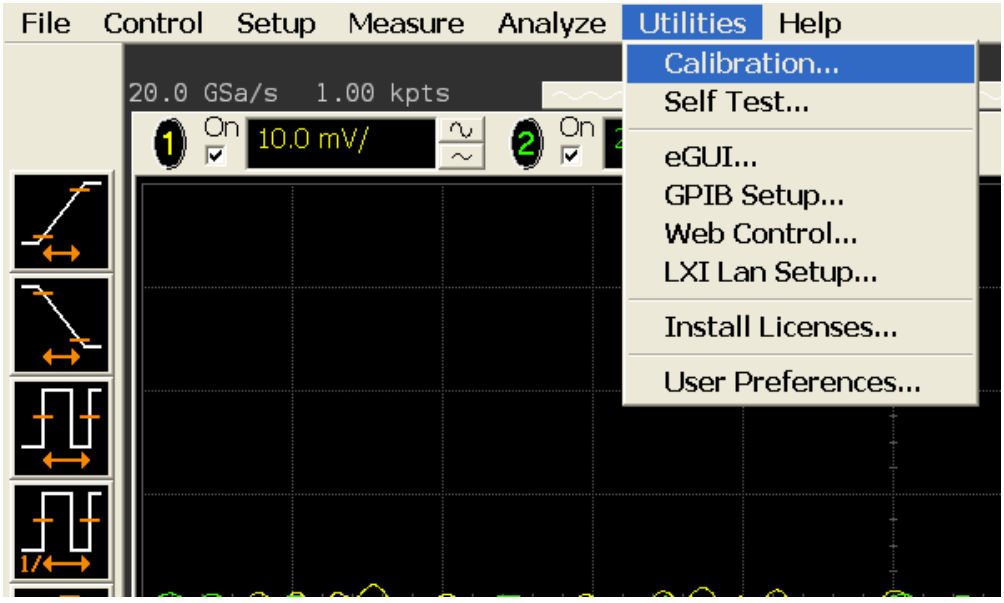


Figure 97 Accessing the Calibration Menu.

4 Referring to Figure 98 below, perform the following steps to start the calibration:

a Uncheck the Cal Memory Protect checkbox.

b Click the Start button to begin the calibration.

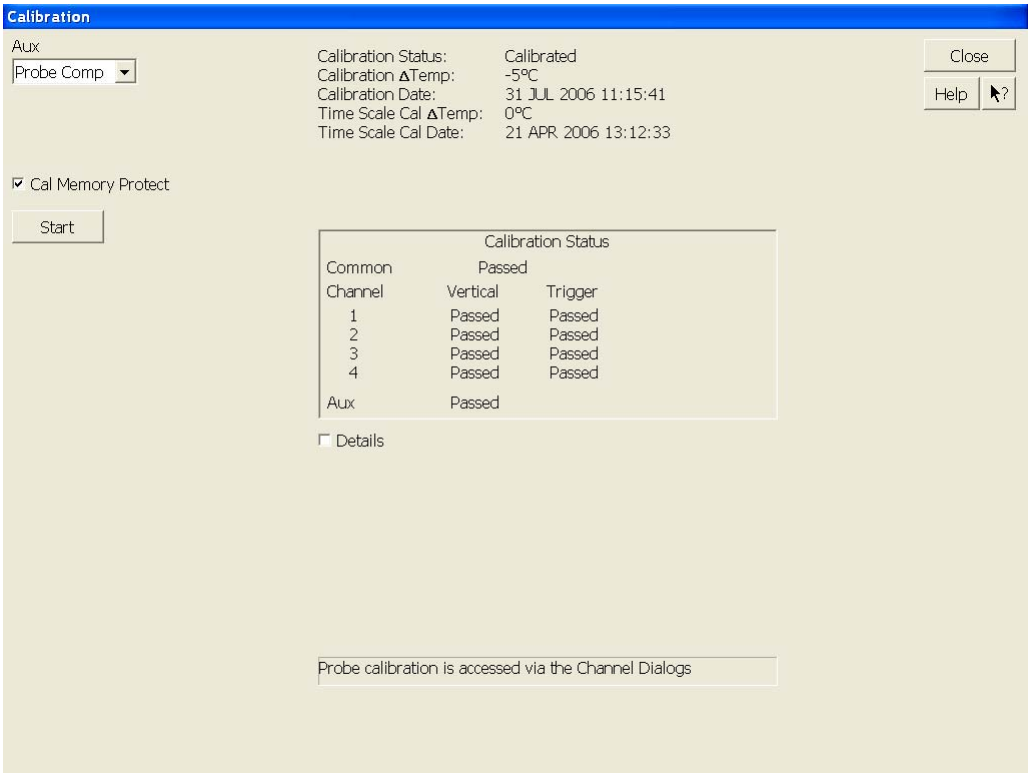


Figure 98 Oscilloscope Calibration Window

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs: click the OK button.

b Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

c During the calibration of channel 1, you will be prompted a Calibration Options screen, as shown in Figure 99 below.

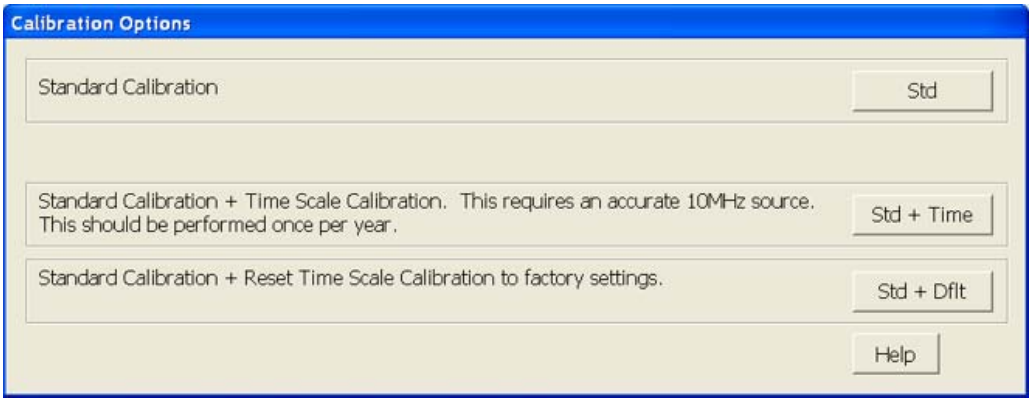


Figure 99 Time Scale Calibration Dialog box

d Click on the Std + Dflt button to continue the calibration, using the Factory default calibration factors.

e When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

f Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

g Click the Close button to close the calibration window.

h The internal calibration is completed.

i Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Probe Calibration and De-skew

Before performing DisplayPort tests you should calibrate and de-skew the probes.

SMA probe head Atten/Offset Calibration

1 Referring to Figure 100 below, perform the following steps:

a Ensure that a probe, attached with SMA probe head is connected to Channel 1. Install the 82 Ω resistors into the SMA probe head. Connect the de-skew fixture to Aux Out. Clip the resistors on de-skew fixture. These resistors are only required for probe calibration and de-skew.

b Click on the **Setup>Channel 1** menu to open the Channel Setup window.

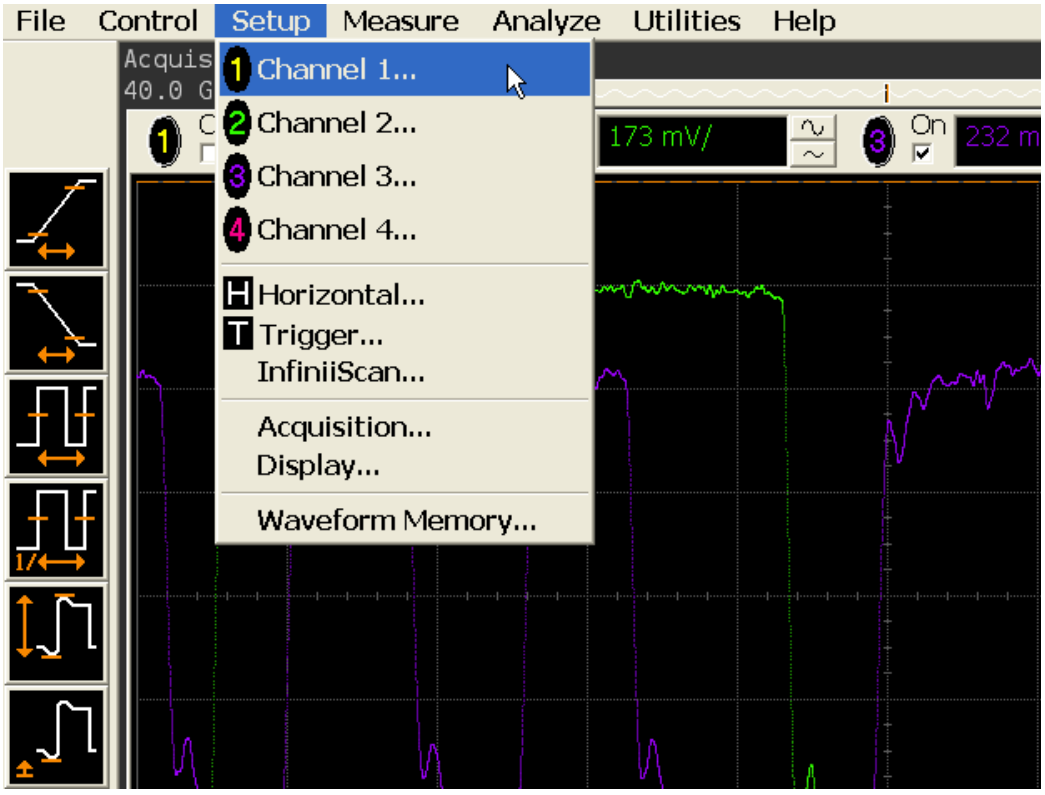


Figure 100 Channel Setup Window.

c Click the Probes button in the Channel Setup window, to open the Probe Setup window.

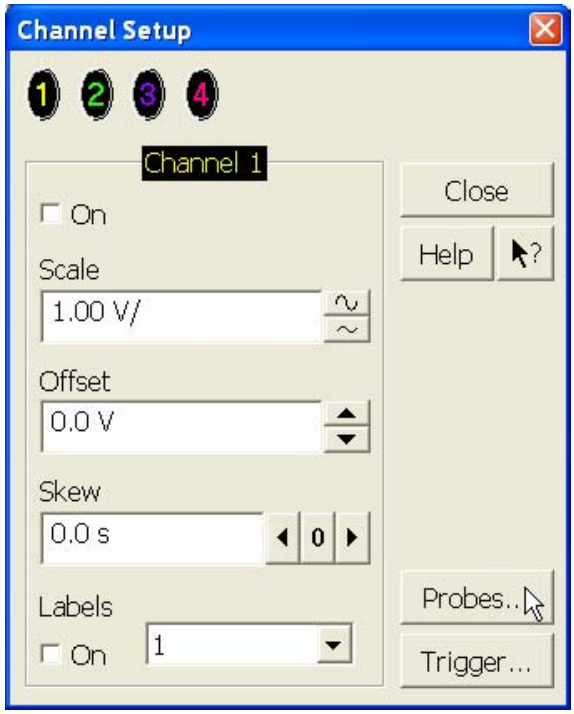


Figure 101 Channel Dialog Box

2 Referring to Figure 102 below, perform the following steps:

a Click the Add Head... button, and then select E2678A:DF Sckt from the list of Head Type. Select OK to close the dialog box.

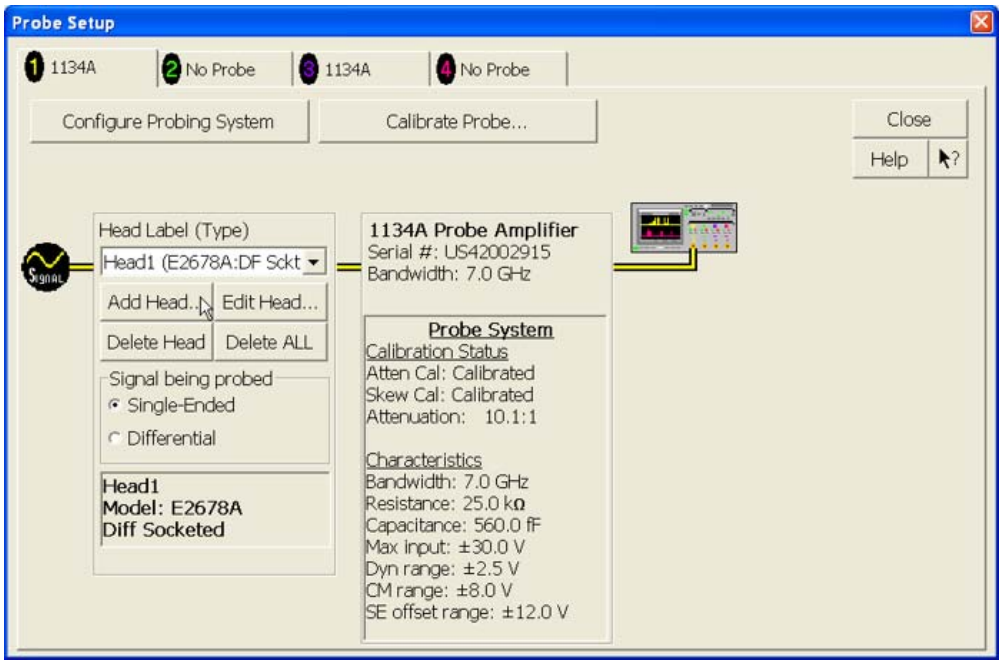


Figure 102 Probe Setup Window.

3 Referring to Figure 103 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

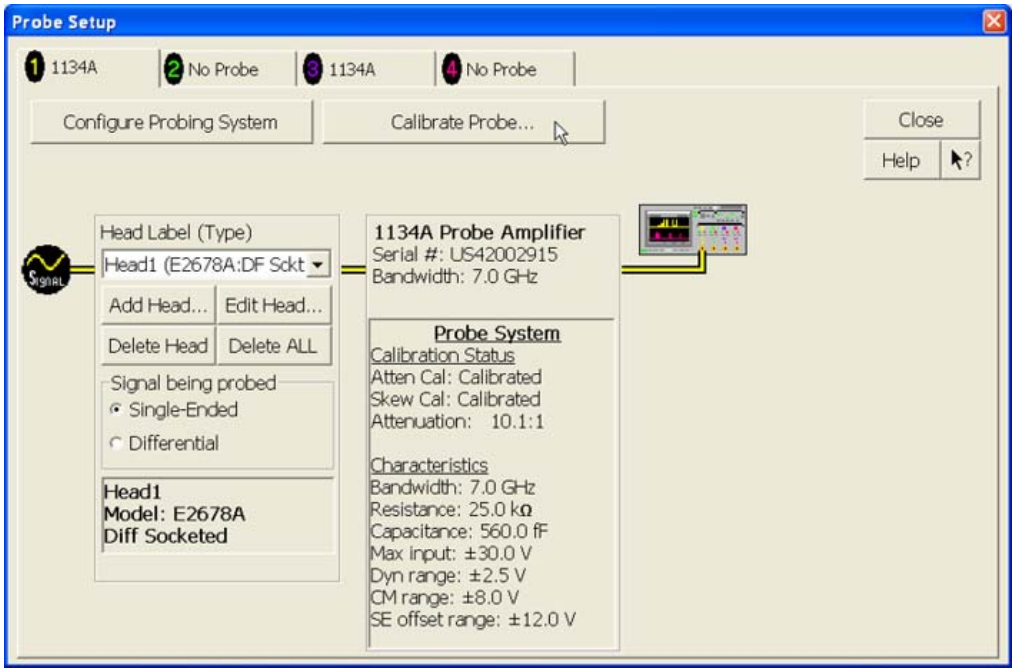


Figure 103 User Defined Probe Window.

4 Referring to Figure 104 and perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

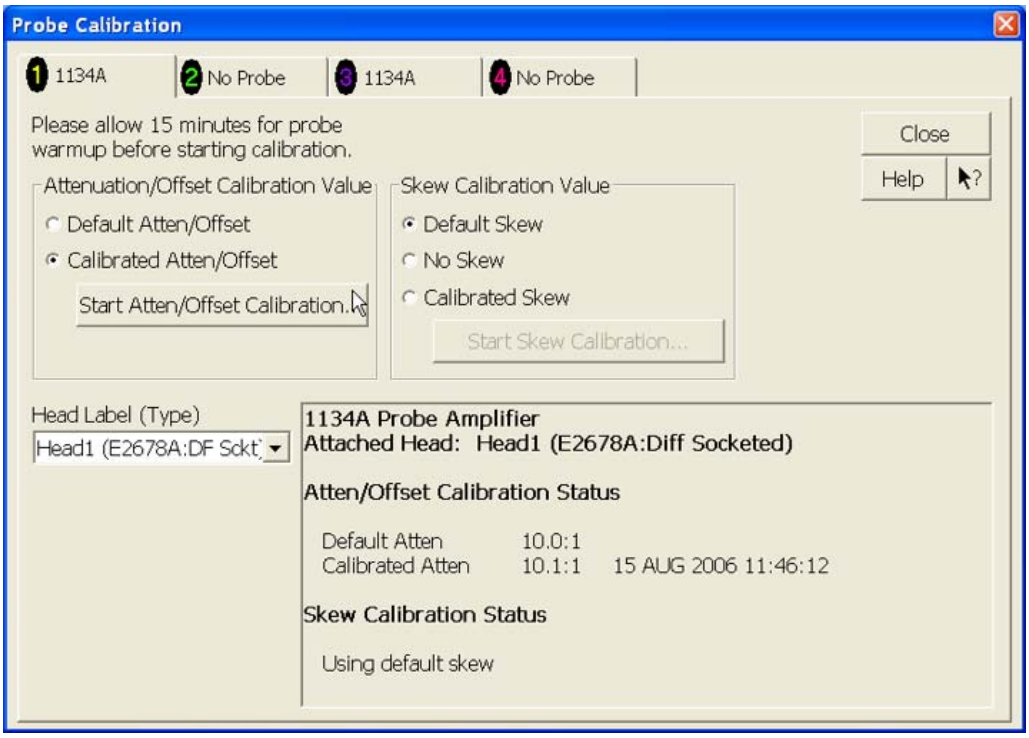


Figure 104 Probe Calibration Window.

c Follow the on-screen instructions.

d At the end of the Atten/Offset Calibration perform the Skew Calibration.

Differential Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

1 Referring to Figure 105 below, perform the following steps:

a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

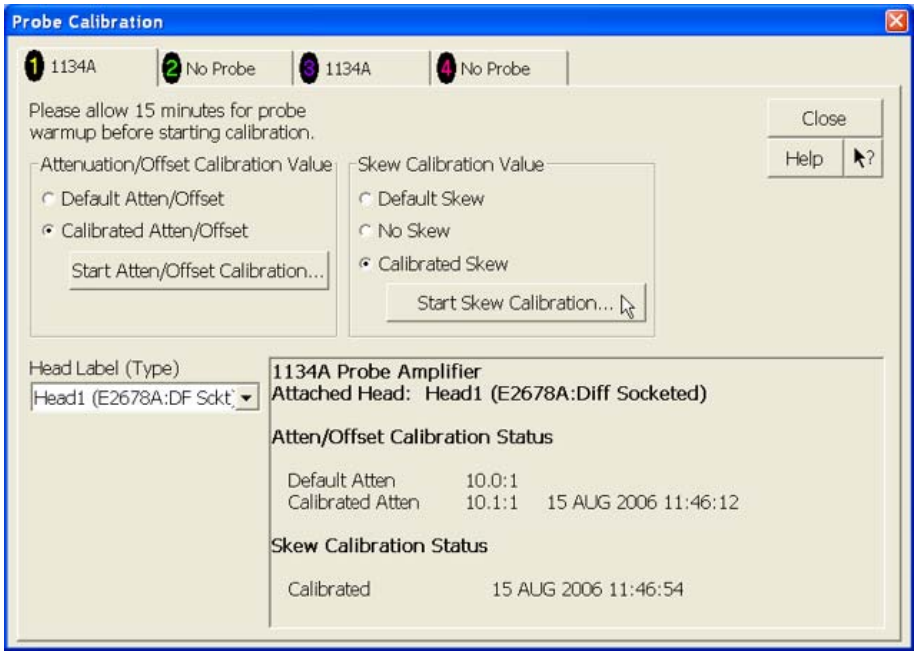


Figure 105 De-skew Connection.

NOTE

Each probe is calibrated to the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes are labeled with the channel on which they were calibrated.

SMA Probe Head Atten/Offset Calibration

1 Referring to Figure 106 below, perform the following steps:

a Connect a shorting cap to the center SMA connector of the SMA probe head.

b Connect the BNC connector of the SMA to BNC adaptor to Aux Out on the front panel of the Infiniium oscilloscope.

c Using the SMA probe head, connect the oscilloscope's Aux Out to the positive (+) side of InfiniiMax probe amp. Connect the negative (–) side to nothing.

Figure 106 SMA Probe Head Calibration

d Click on the **Setup>Channel 1** menu to open the Channel Setup window.

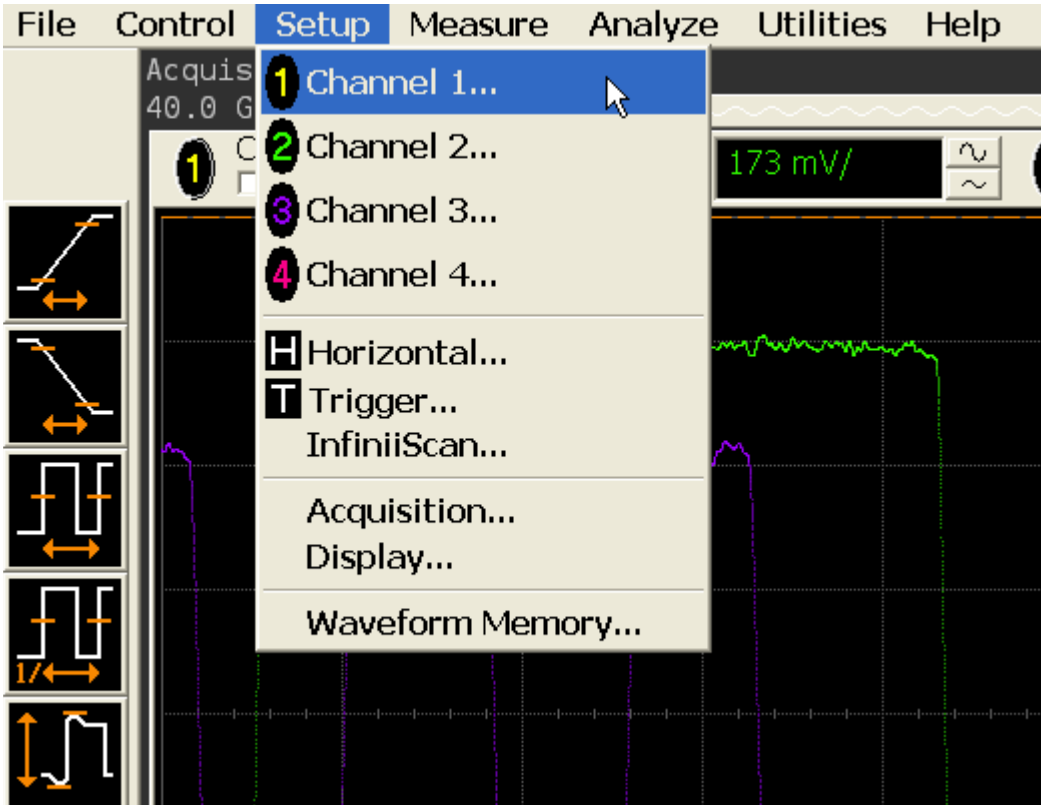


Figure 107 Channel Setup Window

e Click the Probes button in the Channel Setup window, to open the Probe Setup window.

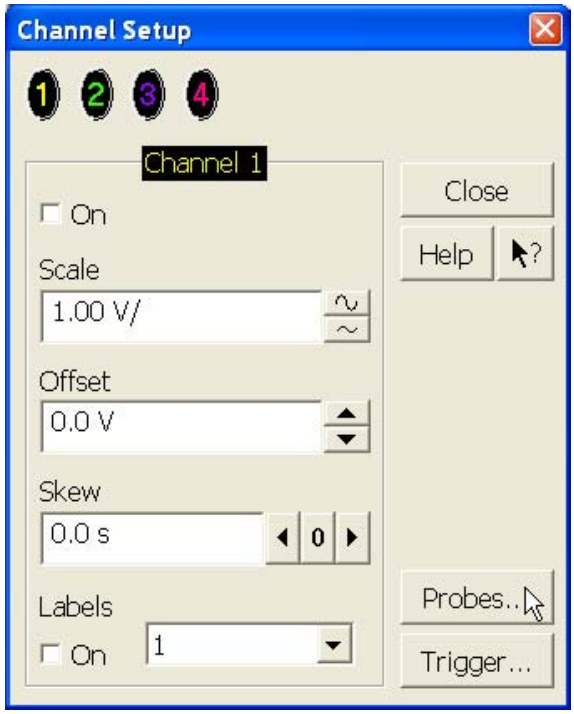


Figure 108 Channel Dialog Box

2 Referring to Figure 109 below, perform the following steps:

a Click the Add Head... button, and then select N5380A:DF SMA from the list of Head Type. Select OK to close the dialog box.

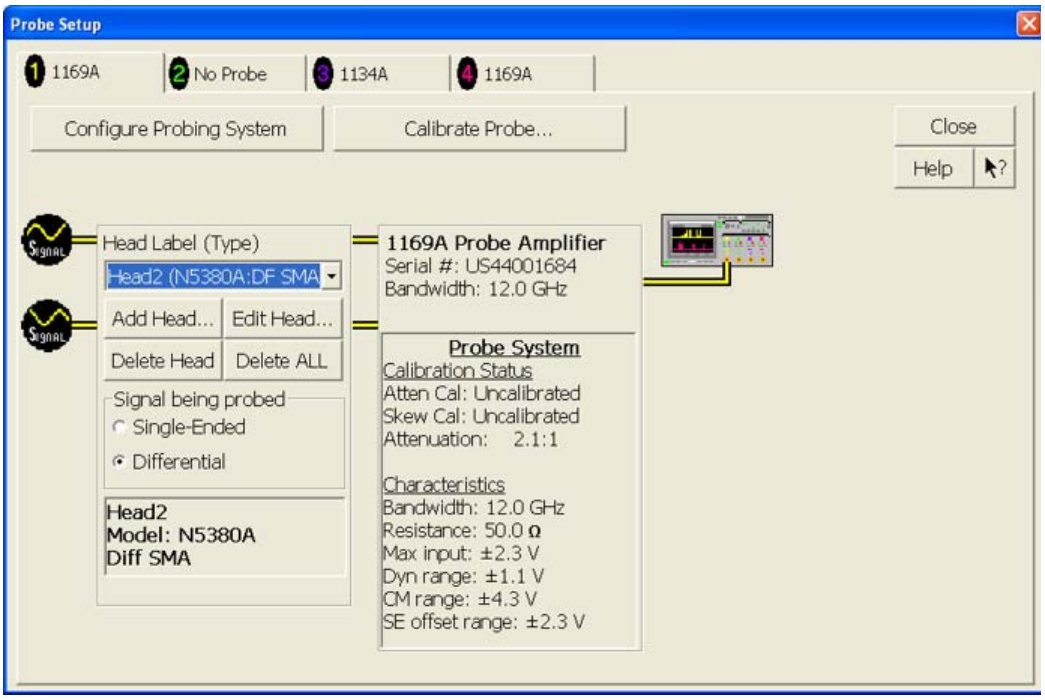


Figure 109 Probe Setup Window.

b Click on the Calibrate Probe button to open the Probe Calibration window.

3 Referring to Figure 110 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

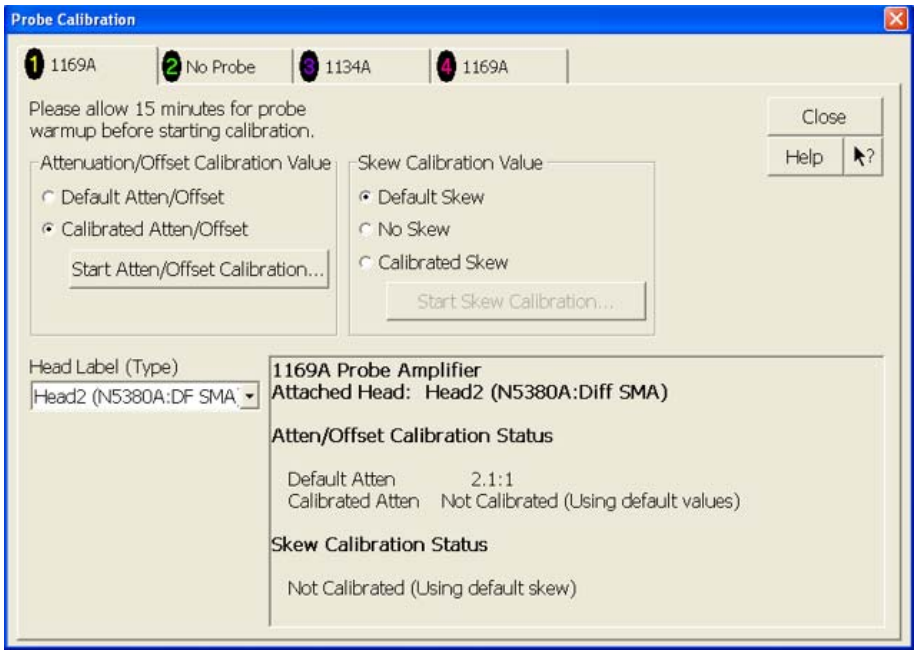


Figure 110 Probe Calibration Window.

c Follow the on-screen instructions.

d At the end of the Atten/Offset Calibration perform the Skew Calibration.

SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

1 Referring to Figure 111 below, perform the following steps:

a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

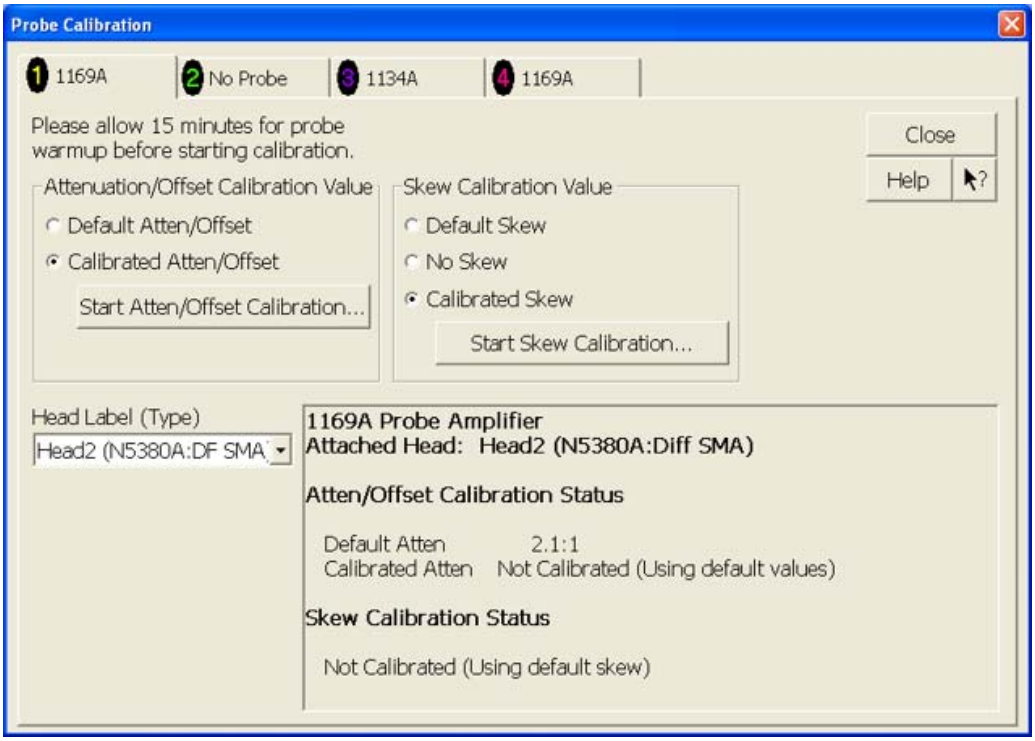


Figure 111 De-skew Connection.

30 InfiniiMax Probing

Figure 112 1169A InfiniiMax Probe Amplifier

Agilent recommends the N5380A SMA probe head and the N5380A differential SMA probe head.

Figure 113 Recommended Socketed Probe Head for the DisplayPort Testing

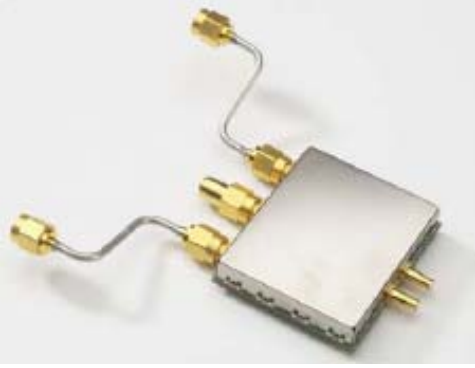


Figure 114 Recommended SMA Probe Head for DisplayPort Testing

Table 35 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential socket	E2678A	7 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm
Hi-BW differential SMA	N5380A	12 GHz	12 GHz

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Seventh edition, March 2011
This part is not orderable.

Version 03.00.0000

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